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Performance Comparison of CMOS and NMOS GNRFET Full Adder

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Abstract: Transistor makes up the cornerstone of modern computing. In this work, a SPICE model of GNRFET was used to simulate the performance of a NMOS and CMOS binary full adder. The performance of this adder was evaluated in terms of its average power consumption and propagation delay. Three variables, namely the resistance value, dimer lines and channel length were manipulated and the impact on its performance was assessed. It was observed that a linear improvement in propagation delay was accompanied by an exponential increase in power consumption and only a small range of values of resistance was able to deliver a relatively reasonable trade-off between power consumption and propagation delay. These values range from approximately 110 kΩ to 130 kΩ. When the dimer lines were varied from 12 to 8 and channel length was varied from 32 nm to 16 nm, the results showed that a channel length of 16 nm was superior to that of a channel length of 32 nm as it showed 25.25 % of improvement in propagation delay at approximately similar power consumption. On the other hand, the choice of dimer lines and circuit architecture was required to be evaluated on a case-by-case basis. For a compute-intensive application with a controlled environment, NMOS logic with 8 dimer lines should be chosen, while for less compute-intensive applications and portable devices, CMOS logic with 12 dimer lines should be utilised. A NMOS logic was chosen for the former due to a reasonable trade-off of 30.94 % of power consumption for a 35.03 % of propagation delay was established When the performance of these full adders are compared to that of a MTGB based ternary gate in terms of their performance, it was found that the CMOS and NMOS logic full adder performed better than a MTGB based ternary full adder.

Keywords: graphene nanoribbon, CMOS, GNRFET, NMOS, propagation delay.

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1. INTRODUCTION

Over the years, transistor scaling has marched at a pace projected by Moore's law, which states that transistor scaling will double every two years. According to International Roadmap of Devices and Systems (IRDS)[1], the key drivers for miniaturisation of transistors include big data and autonomous sensing and computing (IoT). These are technologies which are referred to as More than Moore and these technologies generally demands for chips that have better performance and at the same time consume less power. In order to enable More than Moore applications, it is vital to continue scale-down transistors beyond its scaling limit, therefore, potential future digital logic technologies that expand beyond the present scaling limits need to be studied so that a broadening spectrum of applications can be enabled. These potential future digital logic technologies are referred to as beyond CMOS.

Under the scope of beyond CMOS, recent researches in devices beyond silicon transistors have been focused on graphene which is placed under the category of 2D Material Channel FETs due to its ability to exist as a material which is one-atom-thick without degrading its properties [2]. Graphene has also garnered attention due to its exceptional electronic and mechanical properties such as high flexibility [3], high electron mobility [4], high stability [5], and light-weight [6]. These are the properties which draw researchers to explore the potential of applying graphene for logic operation. In order to allow graphene to serve as a semiconducting material, it has to be made narrow, that is, to form a Graphene Nanoribbon (GNR). This is done by reducing the dimer lines of graphene in an attempt to alter its width. In MOSFET fabrication process, NMOS logic used to be the dominant fabrication process until the invention of CMOS. CMOS, owing to its characteristics such as low static power consumption and high noise immunity [7], has become dominant since then. In fact, as of 2011, 99% of IC chips are fabricated using CMOS technology [8]. In order to investigate the potential of a Graphene Nanoribbon as an alternative material, the performance of a GNRFET based full adder implemented using CMOS and NMOS logic needs to be studied because full adder is the cornerstone in modern digital computing. In research done by Park et al.[11] in 2019, the performance of an 8-bit ALU using 90nm CMOS PTM and 5-trit multi-threshold voltage graphene barristor-based ternary ALU were simulated using HSPICE. The power

delay product of ternary ALU was shown to be lower than binary ALU

In 2018, another research that demonstrated the HSPICE simulation results of adders built from 1-trit 100nm CNTFET,1-trit 100nm graphene barristor and 2-bit 45nm CMOS(PTM) was conducted by Heo et al. [12]. In this research, Monte Carlo Analysis on delay, power consumption and power-delay-product. Among these adders, 100nm Graphene Barristors was proven to have the best performance. Aradhya et al. [13] conducted research in 2016 which presented the design of 10 nm CMOS and GNRFET based 8-bit ALU architecture. These ALUs were simulated using HSPICE and compared. ALUs were implemented using three different types of architecture, namely, 28TFA and NAND-based MUX based ALU, 10TFA and NAND-based MUX based ALU and 10TFA and TG-based MUX based ALU. The architecture with the least heat dissipation was the architecture with 10TFA and NAND based MUX while the architecture with the least delay and the best power-delay product was the architecture with 10TFA and TG based MUX.

Therefore, this study attempt to investigate the potential of a Graphene Nanoribbon Field-Effect Transistor (GNRFET) for use in full adder application. In this paper, a 1-bit full adder using NMOS and CMOS logic based GNRFET was designed. The performance of GNRFET based NMOS and CMOS 1-bit full adder was compared. The performance of the full adders was evaluated based on their propagation delay and average power consumption.

2. METHODOLOGY

In this project, two main circuits were designed and implemented, namely NMOS logic and CMOS logic 1-bit full adder. Simulation of the full adder circuit in HSPICE adopting the SPICE model for GNRFET from Chen et al. [10]. The number of dimer lines used is 12 with a physical channel length of 32 nm and oxide thickness of 0.95 nm. For evaluating the performance of NMOS and CMOS logic full adder, three variables were varied, which included resistance value in NMOS logic full adder, dimer line, and channel length of GNRFET. On the basis of a fixed channel length of 32 nm and a fixed dimer line of 12, the first variable, which was the resistance value of a NMOS logic value, was varied from 10 kΩ to 200 kΩ. The average power consumption, propagation delay, V_{OL} and static power consumption were assessed. The performance of NMOS logic with varying resistance values was benchmarked against CMOS logic full adder with a similar number of dimer lines and channel length. The plot of average power consumption against resistance value would reveal a value that could yield a relatively reasonable power consumption and also V_{OL}. This value was used to examine the effect of varying the width and channel length on the full adders' performance. For both CMOS and NMOS logic-based full adder, average power consumption and propagation delay were measured by changing the channel length from 32 nm to 16 nm while keeping the dimer line constant at 12. Next, the dimer lines of both NMOS and CMOS logic based full adders were altered from 12 to 8. These numbers of dimer lines were chosen as they were reported to have shown different electrical properties [9].

3. RESULTS AND DISCUSSIONS

3.1 Relationship between NMOS Logic Full Adder's Resistance Value and its Performance

The effect of varying the resistance value of the NMOS full adder on its propagation delay, average power consumption and V_{OL} were demonstrated in Figure 1, Figure 2 and Figure 3, respectively. To benchmark, the performance of NMOS full adder against CMOS full adder, the performance metrics of CMOS full adder were represented by a blue line.

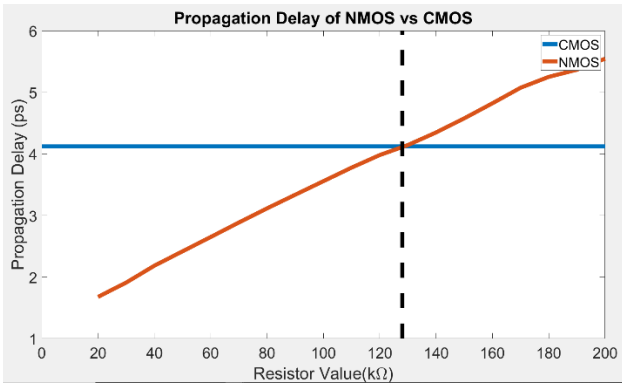

Figure 1. Propagation Delay of NMOS vs CMOS

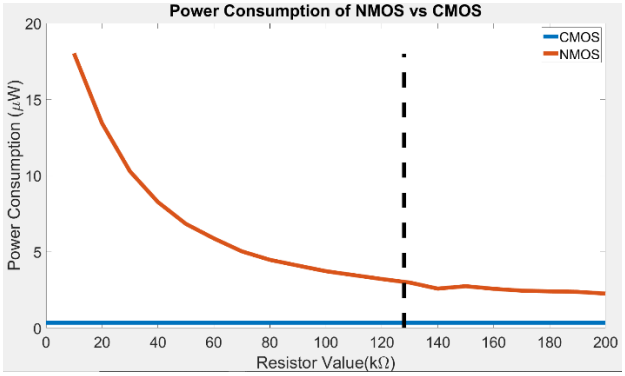

Figure 2. Power Consumption of NMOS vs CMOS

As evident in Figure 2, power consumption exhibited level off and stabilised at approximately 130 kΩ. Despite that, power consumption of CMOS full adder remained superior to NMOS full adder for all resistance values. As a result, to justify the use of NMOS logic solely by its power consumption was not feasible. Consequently, the focus was shifted to analysing the propagation delay of the NMOS full adder.

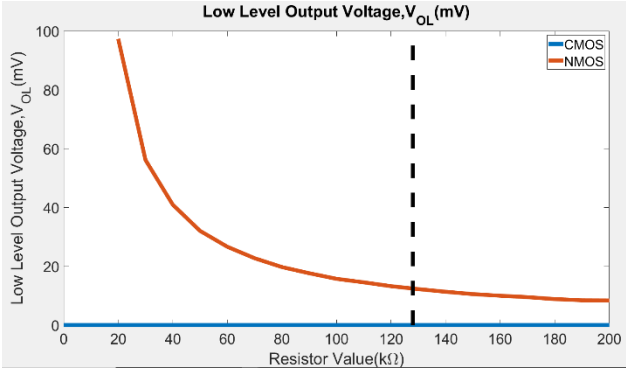

Figure 3. Low-Level Output Voltage, VOL of CMOS vs NMOS

The objective of evaluating the propagation delay of the NMOS full adder was to investigate the possibility of justifying the use of NMOS logic full adder at the expense of higher power consumption. Data in Figure 1 indicated a linear decrease in resistance value was accompanied by a linear decrease in propagation delay. At a resistance value of approximately 130 kΩ, CMOS and NMOS full adder demonstrated a similar propagation delay. This point was marked by a black dotted line. Beyond this point, the propagation delay of NMOS continued to surge in a linear fashion and eventually reached a power consumption five times higher than a CMOS full adder at a resistance value of 200 kΩ. Recalling that power consumption of NMOS was higher than CMOS full adder regardless of the resistance value, it can thus be concluded that there was no solid ground to support the use of NMOS full adder with a resistance value of 130 kΩ and above.

Comparing the propagation delay of a CMOS full adder and an NMOS full adder prior to reaching the resistance value marked by the black dotted line in Figure 2, it can be observed that the propagation delay of the NMOS full adder surpassed CMOS full adder. The propagation delay kept improving in a linear fashion as the resistance value decreased linearly. However, referring to Figure 4.1, the linear improvement in propagation delay was accompanied by an exponential increase in power consumption. As mentioned earlier, in the post-PC era, power consumption is a scarcer resource as compared to propagation delay. A significant compromise in power consumption in favour of an infinitesimal propagation delay seemed unjustified. It can also be seen from Figure 3 the exponential increase in power consumption in NMOS full adder was also accompanied by an exponential increase in low-level voltage output, V_{OL}, whereas for CMOS full adder, owing to the inherent advantage of its circuit design, V_{OL} can be pulled down to zero to achieve a full logic swing. This put pressure on the circuit noise margin and gave rise to issues like crosstalk or deteriorating signal integrity.

3.2 Performance Comparison of NMOS and CMOS Logic Full Adder

In general, a shorter channel length was preferred over a longer one as the transistors could achieve ballistic transport and deliver a more favourable propagation delay with little change in power consumption. However, the choices for dimer lines and circuit architecture are not as straightforward and need to be evaluated on a case-by-case basis. To further evaluate the propagation delay and power consumption of CMOS and NMOS GNR based full adder, the width and length is varied. For this purpose, the resistance value of 130 kΩ was used. The results are presented in Figure 4 and Figure 5. When speed performance is prioritized, a dimer lines of 8 should be chosen and the NMOS logic should be the circuit architecture of choice. Comparing CMOS and NMOS logic with 8 dimer lines, CMOS logic consumes 2.7630 μW of power and has 1.0215 ps of propagation delay while NMOS logic consumes 3.7310 μW of power and has 0.7054 ps of propagation delay. Based on these data, a reasonable trade off of 35.03 % of power consumption for a 30.94 % of improvement in propagation delay is established. All these could be achieved at the expense of lower reliability as the I_{ON}/I_{OFF} ratio is smaller and a large cooling system might need to be attached to the device to make sure the its reliability falls within a reasonable range.

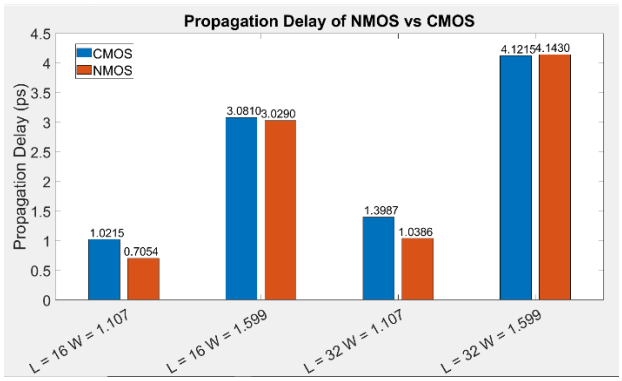

Figure 4. Propagation Delay of NMOS vs CMOS at Different Length and Width

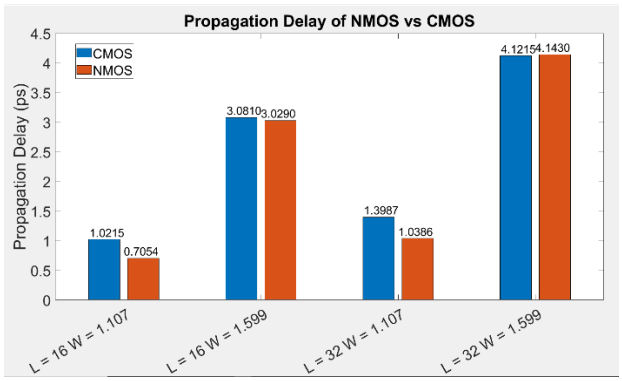

Figure 4. Propagation Delay of NMOS vs CMOS at Different Length and Width

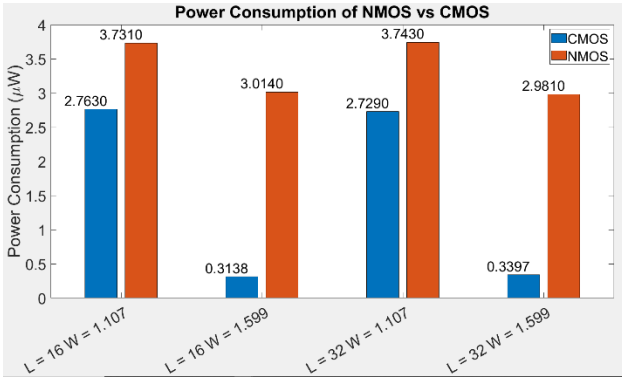

Figure 5. Power Consumption of NMOS vs CMOS with Different Length and Width

Generally, a channel length of 16 nm was preferred over 32 nm for its ability to give 26.97% and 25.25% improvement in propagation delay with little change in power consumption for a CMOS logic with 8 and 12 dimer lines respectively. On the other hand, the choices for circuit architecture and dimer lines required to be evaluated on a case-by-case basis. CMOS logic with 12 dimer lines was identified as the best candidate for low power application due to its reliability and highly favourable power consumption while NMOS logic with 8 dimer lines was identified as the best candidate for compute intensive application which could tolerate a high cost for cooling system and a controlled environment such as super computer or desktop computer with a plugged-in power source due to its speed and also lower reliability. NMOS logic was chosen for the latter because a reasonable trade-off of 35.03 % of power consumption for 30.94 % improvement in propagation delay could be established.

5. CONCLUSION

A GNRFET based 1-bit full adder was designed using both NMOS and CMOS. Functional test patterns were fed to these circuits, and their performances were evaluated in terms of their propagation delay, average power consumption and static power consumption. At a resistance value of approximately 50 kΩ, NMOS logic was consuming 13 times more power while producing only 45.48 % improvement in propagation delay as compared to CMOS logic full adder. A small range of values that was able to deliver a relatively reasonable performance trade-off was identified and was used to evaluate the performance when the dimer lines and channel length were varied. These values range from approximately 110 kΩ to 130 kΩ. It was also observed that the static power consumption of NMOS logic was higher than CMOS. Future work can include the effect of interconnect in the evaluation of the full adder circuit performance based on GNR.

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