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A Five-Level Common-Ground Inverter with Dynamic Voltage Boost and Fewer Elements for Photovoltaic Applications

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Abstract: Transformer-less multilevel inverters (TL-MLIs) are the subject of recent research due to their high-voltage or high-power capacity to convert low-voltage output from renewable energy sources into the desired output. They are also less expensive and smaller than traditional varieties. Nevertheless, leakage current is a common problem with these inverters. The proposed inverter aims to address this issue to the maximum extent possible. In the proposed inverter structure, there is a common ground for the input and output terminals. As a result, the overall common mode voltage (CMV) remains constant. This common ground feature short-circuits the Photovoltaic (PV) source to the grid parasitic capacitor, resulting in negligible leakage current. Furthermore, the proposed inverter boosts output voltage using the least amount of power devices and a single voltage source. The proposed inverter can be used modularly, increasing the number of output levels that can be achieved. The simulation results from MATLAB/Simulink and the conclusion of the mathematical analysis for the proposed inverter are shown. The results also demonstrate the output voltage boost capability, zero leakage current, and an appropriate total harmonic distortion for the output voltage and current waveforms.

Keywords: Boost, Leakage current, Multilevel-Inverter, Single source, Transformer-less

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1. INTRODUCTION

Renewable energy sources, particularly PV, have garnered increased attention in recent decades as vital challenges such as global warming and pollution have evolved. For renewable energy resources, various converters with various structures have been presented. [1]-[4].

Various studies on multilayer converter design have been undertaken, including for solar-based applications in [5]-[13]. This paper explores innovative inverter topologies, modulation approaches, maximum power point tracking systems, and specific PV situations and solutions. Furthermore, the fundamental goal of these topologies is to build inverters with low leakage current.

Inverters with switched capacitors (SC) or switched inductors (SI) have recently been devised to achieve a higher output voltage gain. This feature enables the inverter to convert low input voltage sources to the desired output voltage for grid-connected applications. Recent research has been conducted to increase the voltage gain of Neutral Point Clamped (NPC)--based inverters by using switched capacitors [14]-[22]. To increase the output voltage, the switched capacitors are exhausted in series with the DC link capacitor in these converters.

The presence of current spikes while charging the capacitors is a concern in the majority of these NPC types of inverters. As a result, the studies in refs [23]-[24] are proposed to address this issue. These studies offer new active NPC-based structures that can enhance voltage. The maximum voltage gain, on the other hand, is increased to twice the input voltage value.

To avoid further losses in two-stage transformer-less inverters, the dual-mode time-sharing method has been proposed in several studies [25]– [29]. When the PV voltage is less than the grid voltage, the boost stage will kick in. Pourfaraj et al. and Kakar et al. [25]-[26] provide a dual-mode transformer-less interleaved multilevel inverter with an interleaved boost converter. The main contribution of these inverters are lower current stress across semiconductors and DC-side inductors. Also, the main limitation is the necessity of a comparatively higher number of semiconductors and the presence of high-frequency components on the common mode voltage (CMV). The fault-tolerant (FT) capability is one of the important features of multilevel inverters to keep supplying the output load in various fault conditions to increase the reliability of the inverter. A single-phase PV converter with a common ground and three switches is proposed to supply reactive electricity to the AC grid by Heydari-doostabad et al. [27]. The inverter's advantages include low noise, regulation of active and reactive power, step-down and step-up output voltage, and low A 5-level common ground type (5L-CGT) inverter with two times

the voltage gain is proposed by Anand et al. [28]. Unfortunately, boost operation with a variable duty cycle is out of the question with this inverter. In [29], Wang, Shan, et al. offer a non-electrolytic capacitor for use in a single-stage, common-ground zeta inverter. This inverter solves problems with electrolytic capacitors, common mode (CM) leakage current, and voltage boosting or dropping.

In conclusion, an inverter must have a multilevel structure that gets rid of common mode voltage (CMV), has no leakage current, and can work even when something goes wrong. Additionally, this inverter should possess a boost voltage gain feature. Such a design is essential to achieve a safe and dependable inverter that is well-suited for low-voltage renewable applications.

This paper proposes a novel five-level boost inverter with continuous gain control capability. The input side of the proposed inverter is supplied by an inductor, so a continuous input current has been supplied to the input source, making the inverter appropriate for PV and other renewable energy applications requiring DC or AC operation. In addition, the improved levels of the inverter for a seven-level operation have been provided to demonstrate the inverter's modularity. In addition, the number of components is small, and the leakage current is close to zero as the negative end of the power source is wired directly to the neutral terminal of the grid.

The following is how the paper is structured: Section 2 describes the structure of the proposed 5-level multilevel boost inverter. Section 3 describes the process and scheme for generating switch pulses. Section 4 contains MATLAB Simulink results for an inverter. Finally, Section 5 has the conclusion.

2. PROPOSED MLI STRUCTURE

This section discusses the exceptional benefits of the proposed 5-level inverter. Figure 1 illustrates the proposed five-level circuit. In the proposed design, a boost inductor is used to provide continuous input current and facilitate voltage gain that can be controlled. Using a single DC source, the converter with the appropriate specifications for PV applications is developed. Additionally, the inverter is modular and contains fewer controls. The proposed inverter has a substantially high boost gain, and the peak output voltage can be calculated as 2M/(1-D) and 3M/(1-D) for 5-level and 7-level output voltage levels, respectively.

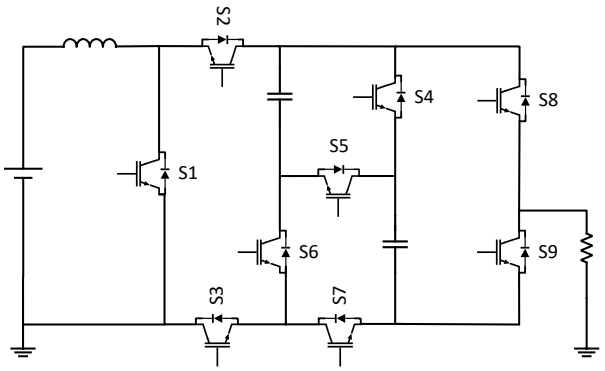
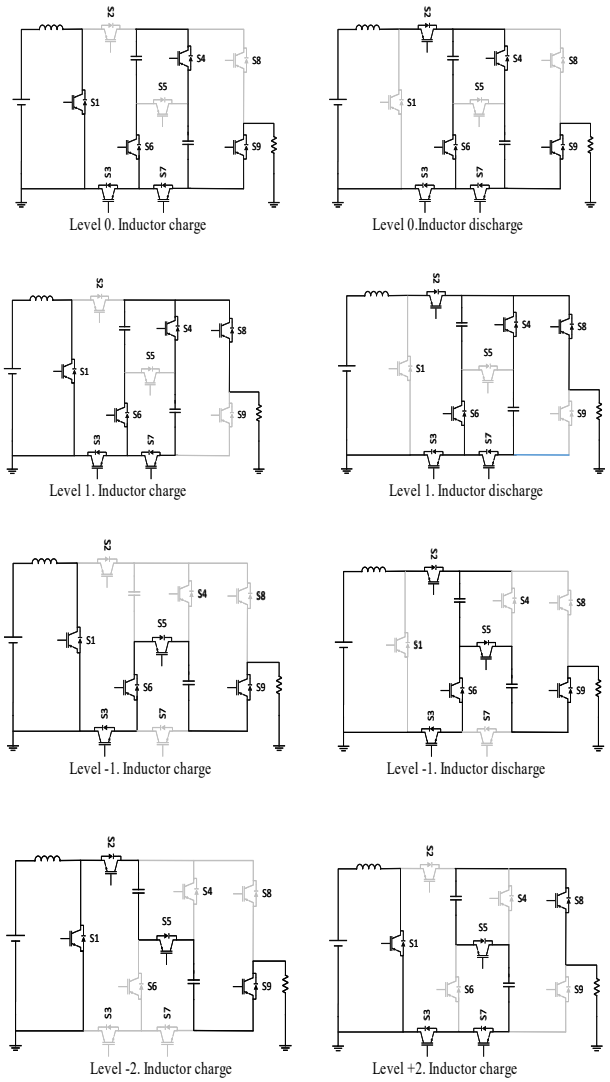


Figure 1. The proposed 5-level inverter structure

2.1 Operating Modes

In this section, Figure 2(a), shows the main operating modes of the proposed 5-level converter. These modes provide replacement working modes for each voltage stage so that the output voltage stays the same when there is a problem. Each phase of operation incorporates both the charging and discharging phases of the input boost inductor. In addition, the implementation includes a variety of charging and discharging states for varying inverter output levels. In addition to balancing the voltage of capacitors and simplifying the control of the boost duty cycle, this feature provides additional benefits, such as voltage balancing for capacitors.

In addition, this inverter's input inductor is charged when the IGBT S1 is ON and discharged when the power switch S1 is OFF. So, the key waveforms of the proposed inverter have been demonstrated in Figure 2(b).



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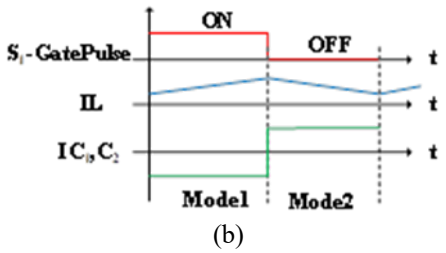


(b)

Figure 2. (a) Different operating modes of the 5-level converter and (b) Key waveforms of the inverter in charge and discharge operations

2.2 Essential mathematical calculations

The proposed inverter uses a specific approach to obtain modulation index values between zero and maximum. The following is an expression for the maximum DC gain:

$$Gi = \frac{2M}{1-D} \tag{1}$$

In the proposed inverter, the capacitors have been charged to the same value, and the corresponding voltage of each capacitor can be obtained as:

$$V_{C1} = V_{C2} = \frac{V_{DC}}{1-D} \tag{2}$$

Consequently, the maximum peak voltage is equivalent to the summation of the voltages present on the mentioned capacitors. Therefore, it can be obtained as:

$$V_{O,Max} = \frac{2V_{DC}}{1-D} \tag{3}$$

The following equations in Table 1 illustrate the association between the output voltage and modulation index. The duty-cycle (D) variations can change the output voltage peak value. Table 2 demonstrates the peak output voltage value variations. For the modulation indexes higher than 0.5, due to the Level shift PWM (LS-PWM) strategy employed, the inverter output will have a 5-level waveform based on a sinusoidal reference voltage signal. Also, for M<0.5, the converter output will be changed to 3-level.

Table 1. The relationship between the modulation index and the output voltage

Output Voltage	Modulation Index Range	Output Voltage Range
$V_O = \frac{2MV_{DC}}{1-D}$	0 to 1	$V_O => 0\ to\ \frac{2V_{DC}}{1-D}$

Table 2. Application of the proposed method and the resulting output voltage gain for different modulation index ranges

Modulation Index	Possible Output levels	Output Voltage peak gain
M>0.5	5 Levels	$\frac{V_{O,peak}}{V_{DC}} = \frac{2}{1-D}$
M<0.5	3 Levels	$\frac{V_{O,peak}}{V_{DC}} = \frac{1}{1-D}$

2.3 Design considerations

This section presents the proposed inverter design considerations for the power switches, input boost inductor, and capacitors. As shown in the accompanying equations, equations representing the voltage stress of the power switches are derived.

$$V_{4,6} = \frac{1}{1-D}V_{DC}, V_{S1,2,3,5,7,8,9} = \frac{2}{1-D}V_{DC} \tag{4}$$

Also, the input boost inductor can be designed by the following equation:

$$L_{in} \geq \frac{DV_{DC}}{f_s \Delta i_L} \tag{5}$$

Moreover, the inverter capacitors values can be defined as follows:

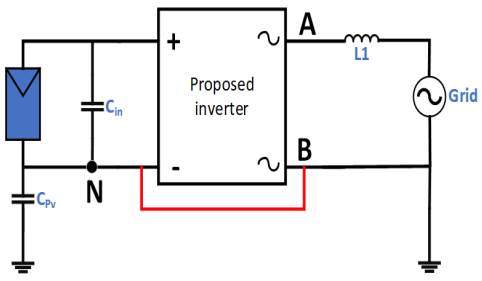
$$C_{1,2,\ldots n} \geq \frac{D(1-D)I_o G}{f_s \Delta V_C} \tag{6}$$

3. METHODOLOGY

The suggested inverter construction eliminates leakage current for PV to grid applications and creates a common ground between the input and output sides, resulting in a zero CMV. The voltage between point B and neutral point N (V_{BN}=0) is equal to zero, as shown in Figure 3(a). Thus, taking this number into account, the inverter's total common mode voltage can be expressed as follows:

$$V_{CM.Total} = \frac{V_{AN}}{2} + (V_{AN})\left(\frac{-L_1}{2(L_1)}\right) = 0 \tag{7}$$

This means that the CMV as a whole is zero. Additionally, Figure 3(a) indicates that the PV's parasitic capacitor (C_{PV}) is short-circuited. Consequently, there is no leakage current via C_{PV}. Additionally, the suggested inverter can operate continuously as a boost operation, enabling it to get a wider output voltage range for input voltage sources that are lower.



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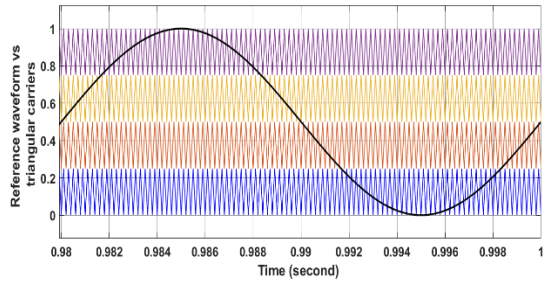


(b)

Figure 3. a) The general schematic of the proposed inverter connection to the AC grid, b) The waveform of the triangular carrier signals in comparison with the reference sinusoidal waveform of the proposed inverter.

3.1 Modulation and Switching Rules

The suggested structure drives the IGBTs using the level shift modulation technique to produce a sinusoidal waveform at the output. Figure 3(b) displays the carrier signal waveforms in comparison to the reference sinusoidal waveform. Four triangular carrier waveforms will be present in a 5-level inverter. There is at least one scenario for inverter switching for every voltage state. Because of this, Table 3 describes the switching table for the suggested inverter, which takes into account five levels ranging from -2V to +2V. The converter is adaptable for fault-tolerant applications due to the range of switching strategies available for each voltage state.

Table 3. The switching conditions for the proposed 5-level inverter

Level/ Switches	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	**Inductor**
0	1	0	1	1	0	1	1	0	1	Charge
	0	1	1	1	0	1	1	0	1	Discharge
+1	1	0	1	1	0	1	1	1	0	Charge
	0	1	1	1	0	1	1	1	0	Discharge
-1	1	0	1	0	1	1	0	0	1	Charge
	0	1	1	0	1	1	0	0	1	Discharge
-2	1	1	0	0	1	0	0	0	1	Charge
+2	1	0	1	0	1	0	1	1	0	Charge

3.2 Modular operation of the inverter

The modular operation capabilities of the suggested inverter allow it to be configured to increase both its peak voltage gain and the number of output voltage levels. Figure 4 in this section depicts the 7-level structural topology that was obtained from the suggested circuit.

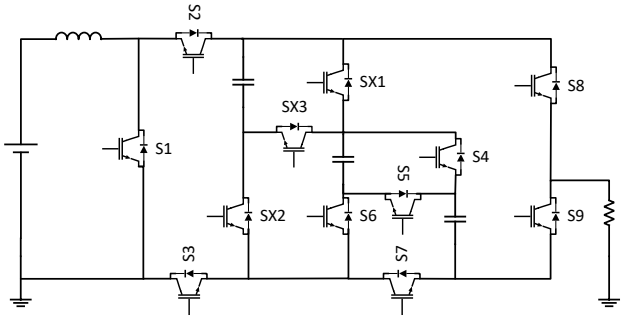


Figure 4. The 7-level structure topology based on the proposed circuit

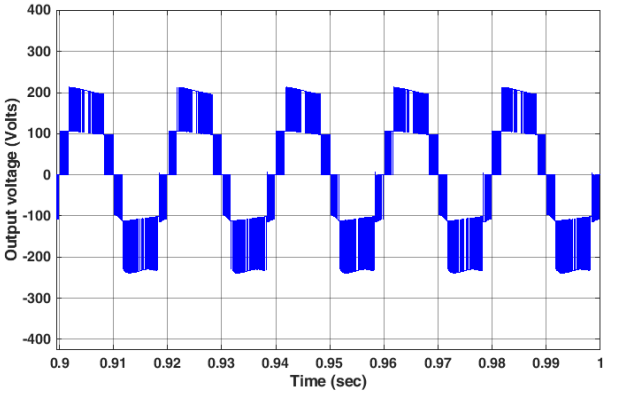
4. RESULTS AND DISCUSSION

The suggested inverter can function as a continuous boost mode, continuous input current, common ground mode with zero leakage current, and 5-level output voltage for the output load, in accordance with the sections that came before it. The main software results from MATLAB/Simulink are shown in this part, along with confirmation that the converter is feasible. To illustrate the percentage of losses for each inverter component, the data have also been supplemented with the comprehensive loss analysis result from the PLECS software simulation. The critical parameter values for the inverter employed throughout the simulation are displayed in Table 4. Lastly, Table 5 provides a comparison of the suggested inverter with other architectures. With a peak value of 210 V, the output 5-Level voltage is depicted in Figure 5(a) by taking into account the parameter values in Table 5, which is consistent with the formulae in Table 2.

Figure 5(b) illustrates the output voltage in order to demonstrate the continuous voltage variations with duty-cycle modifications. The duty cycle has been adjusted in this figure in 10% steps, from D=80% to D=20%. One advantage of the suggested inverter is its ability to regulate the output voltage's peak value within the expanded operation area. Additionally, the modulation index value in Figure 5(c) has been adjusted from 0 to its maximum value (M=1). The inverter generates a 3-level output voltage when M<0.5, and a 5-level waveform when M>0.5, in accordance with Table 2. Additionally, Figures 6(a) and 6(b) show the voltage waveforms of the inverter capacitors (C1 & C2).

Table 4: The key parameter values for the proposed inverter simulation

Parameter	Value	Parameter	Value
Input voltage (V_{dc})	24 V	Input inductor (L_b)	3mH
Capacitor values (C_1 and C_2)	1200µF	Output load	100Ω + 10mH
Switching frequency	10 kHz	PWM	Level Shift PWM
Modulation Index (M)	1	D	80%



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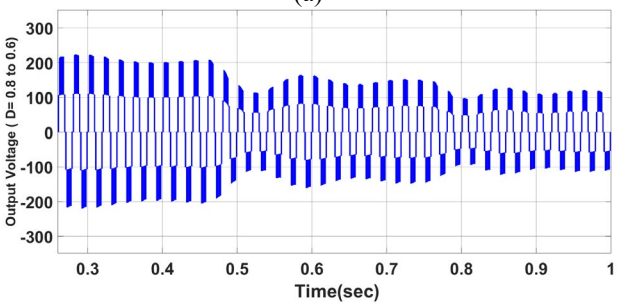

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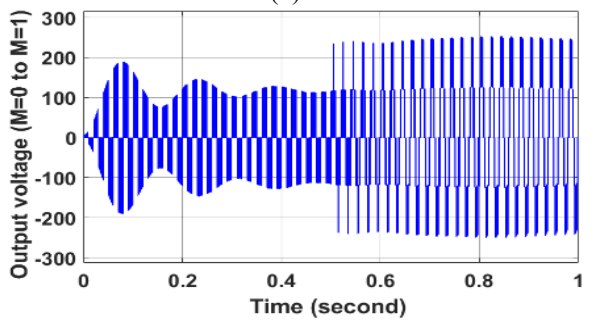
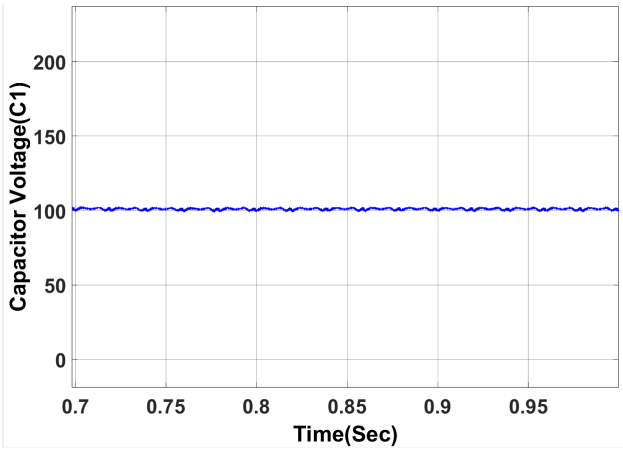


(c)

Figure 5. Output voltage waveforms: (a) Output voltage waveform (D=80%, M=1), b) Sweeping the duty-cycle from D=80% to D=20, (c) Sweeping the modulation index from M=0 to M=1.



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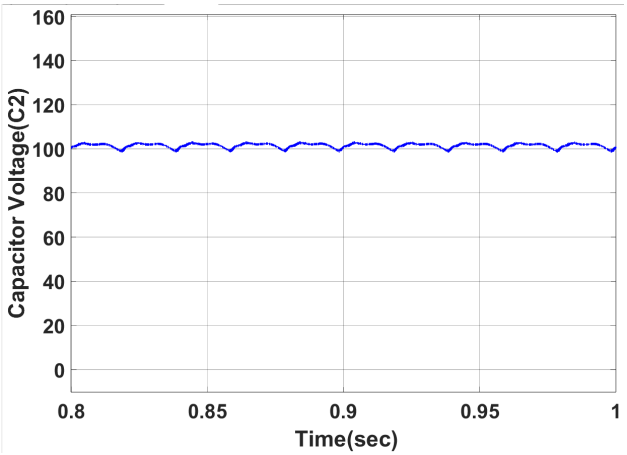
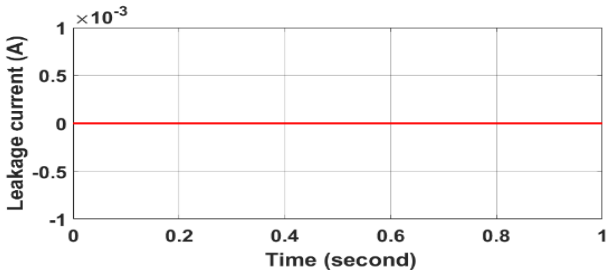


(b)

Figure 6. Voltage waveforms of the inverter capacitors, a) VC1 and b) VC2

Figure 7(a) shows that there is no leakage current across the parasitic capacitance of the input source. Additionally, Figure 7(b) displays the output current waveform of the inverter with the previously described properties in Table 4. In addition, Figure 8(a) shows that the inverter output voltage and current have Total Harmonics Distortion (THD) values of 27.10% and 0.65%, respectively.



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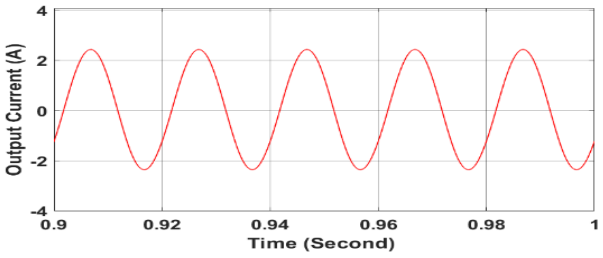
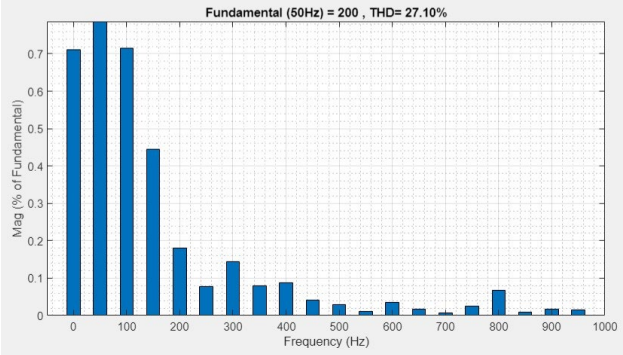


(b)

Figure 7. (a) Leakage current waveform, (b) Zoomed output current waveform



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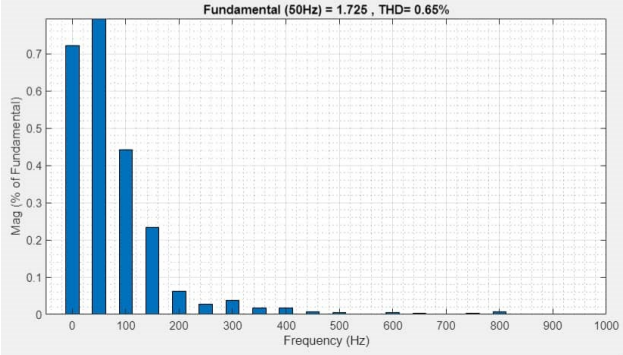
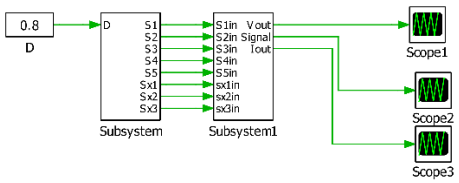


(b)

Figure 8. The harmonic spectra and THD of the inverter, (a) output voltage (b) output current.

4.1 Inverter Comparison and Losses Analysis

This section presents a comparison with other innovative structures with the suggested 5-level and 7-level inverters. Table 5 shows that the suggested inverter is more suited for PV and renewable energy applications due to its higher voltage gain with continuous input current. Additionally, the modular operation of the inverter yields better boost voltage gains. Furthermore, figures 9(a) and 9(b) show the simulated converter. A comparison of voltage gain is additionally shown in Figure 10(a). Additionally, Figures 10(b), 10(c) display the loss distribution between the inverter's component parts in percentage and the converter's efficiency curve when the output power is varied from 0 to 1500 Watts under real conditions based on the values in Table 6.



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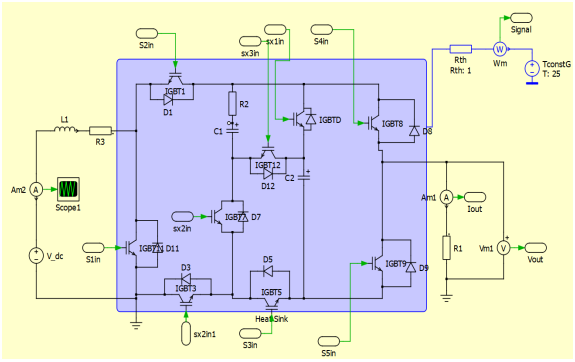


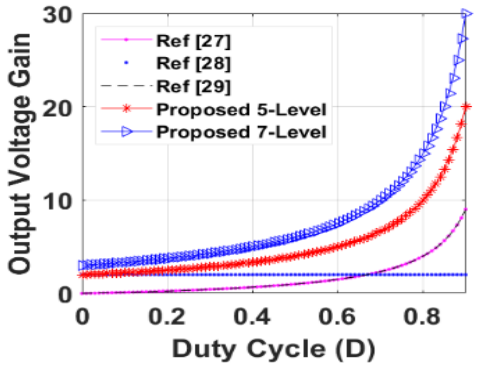
(b)

Figure 9. The simulated converter with PLECS software, a) control system, b) proposed converter

Table 5. Comparative analysis of the proposed structure and its comparable topologies

Structure	N_S	N_{Diode}	N_{Cap}	N_L	N_{Level}	Gain	CC	CG
[27]	3	6	2	2	3	$\frac{DV_{dc}}{(1-D)}$	×	✓
[28]	7	0	2	1	5	$2V_{dc}$	×	×
[29]	6	3	2	1	3	$\frac{DV_{dc}}{(1-D)}$	×	✓
Proposed 5-level	8	0	2	1	5	$\frac{2MV_{dc}}{(1-D)}$	✓	✓
Proposed 7-level	11	0	3	1	7	$\frac{3MV_{dc}}{(1-D)}$	✓	✓

*N_S: Switches count, N_{Diode}: Diodes count, N_{Cap}: Capacitors count, N_L: Inductors count, N_{Level}: Number of voltage levels, Gain: Voltage boost gain, CC: Continuous input current, CG: Common ground and M: Modulation index.



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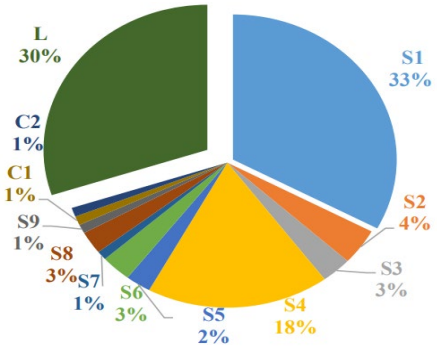

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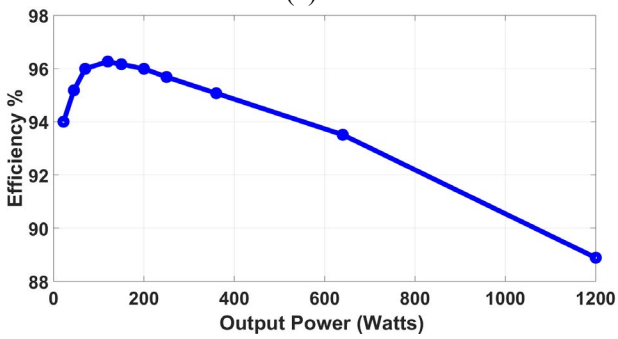

(c)

Figure 10. The voltage gain comparison and loss analysis of the proposed inverter: (a) output voltage gains vs duty cycle, (b) loss per component, and (c) efficiency curve

Table 6. Elements and parameters used to compute losses and efficiency

Parameter	Value	Parameter	Value
Power Switches	IGBT-FGH60N60SMD	Input Voltage	24V
Input Inductor	3mH (10mΩ internal resistor)	Duty-Cycle (D)	80%

5. CONCLUSION

A novel multilevel boost inverter with a non-pulsating current at the input has been developed in this work to use it in photovoltaic and other renewable energy systems. The several switching strategies for each output voltage level of the suggested inverter have been demonstrated, offering benefits like simple duty-cycle management and capacitor voltage balancing. Furthermore, the 5-level structure's boost gain is doubled (2D/1-D) while the 7-level structure's boost gain is tripled (3D/1-D). The inverter's mathematical analysis has been emphasized, and the suggested structure has been contrasted with other recently developed, pertinent structures. Lastly, the simulation results for the MATLAB/Simulink environment have been supplied to show the effectiveness of the inverter.

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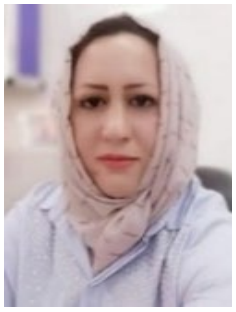

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