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Integrated Self-Test Module for Uncorrelated Photon Counting in a Two-Dimensional Array

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Abstract: A 16 × 2 two-dimensional (2-D) array of single-photon avalanche diodes integrated in a complementary metal-oxide-semiconductor (CMOS) process is presented. Each pixel is made up of an avalanche photodiode biased in the so-called Geiger mode, a quenching resistor, and a basic comparator. To implement the photon counting verification on the chip, a build-in-self-test (BIST) module is added. Full integration allows for 10218.70 μm^2 of total cell area and 1.7837 mW of power consumption, which is about 38% less than the 2.8567 mW of the prior design. The circuit is capable of running at a 200 MHz counting rate. The array's internal signals and status can be monitored while it is being tested or used thanks to the built-in logic block observation module demonstrated in this paper. The effectiveness and efficiency of testing can be increased, as well as the performance of the readout electronics, by adding Kogge-Stone adder and BIST circuits to the array design. The ability to quickly adapt the design to suit a particular application is another undeniable advantage of CMOS integration, which also paves the way for on-chip data processing.

Keywords: Built-in self-test (BiST), avalanche photodiode

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1. INTRODUCTION

Uncorrelated photon counting records the time of arrival of each individual photon without attempting to relate it to any other event or pulse. A photon count histogram is created by counting the number of photons that pass through the detector during a specific window of time. This method is frequently applied in situations where the time-resolved behavior of the light is unimportant, such as fluorescence intensity measurements [1], [2]. The signals produced by individual photodetectors in an array are read out and processed by a circuit known as a readout circuit for a photon counting array. These arrays are frequently used in single-photon detection and imaging applications where it is important to precisely detect and measure individual photons [3], [4]. Light Detection and Ranging (LiDAR), medical imaging, and quantum communication are a few examples of applications that use photon counting array data processing on the chip. However, a self-test module is necessary to guarantee the precision and dependability of the data generated by the chip. Various tests are run by the self-test module of the photon counting array data processing chips to find and fix data errors. It ensures the proper operation of the signal-processing algorithms, the functionality of the analog and digital circuits, and the accuracy of the photon detector's integrity. Without a self-test module, errors in the chip's data may go undetected, resulting in inaccurate results and possibly disastrous outcomes.

Preamplifiers, amplifiers, discriminators, and counters are frequently found in the readout circuit for a photon counting array. Each of these elements has a particular function in recognizing and handling individual photon signals. The weak signals produced by the array's photodetectors are amplified by preamplifiers. It often takes an amplifier to accurately detect and process these signals because they are frequently very small. Amplifiers are used to strengthen preamplified signals so they can be precisely measured [5]. Discriminators are used to separate noise pulses from other sources from signal pulses produced by individual photons. Thus, discriminators only count pulses that exceed the threshold in order to determine whether a pulse is a true signal or not. The number of signal pulses identified by the photon counting array is counted using counters. These counters provide a way to gauge the strength of the photon flux and can be implemented using a variety of digital logic circuits. In general, a photon counting array's readout circuit is a key element in the precise detection and measurement of individual photons. The readout circuit is capable of processing the weak signals produced by the photodetectors and offering a precise estimation of the photon flux intensity through the use of preamplifiers, amplifiers, discriminators, and counters [3].

As these two requirements are frequently at odds with one another, designing a photon-counting array that can achieve both high data rates and low energy consumption is a difficult task. To achieve high data rates, the readout circuit of the photon counting array needs to be able to process a large number of individual photon signals per second. This typically requires high-speed electronics and complex signal processing algorithms that can quickly distinguish between true and noise signals. At the same

time, to achieve low energy consumption, the readout circuit needs to be designed to minimise power consumption as much as possible. This can be done through a number of different techniques, such as using low-power transistors, reducing the clock frequency of the electronics, and optimising the signal processing algorithms to minimise the number of operations required. To balance these conflicting demands, designers of photon counting arrays often use a number of different approaches. One common approach is to use parallel readout circuits, where multiple readout circuits are used in parallel to process different segments of the photon counting array. This can help to increase the overall data rate of the system, while also allowing each readout circuit to operate at a lower clock frequency and consume less power. Another approach is to use custom-designed integrated circuits that are optimised for low-power operation. These circuits can be designed specifically to meet the requirements of the photon counting array and can include features such as low-power amplifiers, digital signal processing units, and specialised power management circuits [6].

Suhaila et al. presents the significance of Single-Photon Avalanche Diode (SPAD) in a 16 × 1 array in order to enable the potential for imaging [3]. To make the photons detected by the SPAD array countable and observable, a readout circuit will be needed. Two key components make up a complete parallel photon counting circuit: the front-end SPAD array that detects asynchronous photon signals and the back-end synchronous data acquisition system [7, 8]. The design of a small, two-dimensional SPAD array with CMOS integration is described in this paper. It includes active quenching circuit pixels and read-out electronics. The digital readout circuit is intended to provide the precise and trustworthy measurement of photon emissions from the input signal. It also features a self-testing mechanism that can identify and report any operational flaws or errors. The key characteristics are then presented, including the probability of normal mode and scan mode.

2. CIRCUIT DESIGN DESCRIPTION

The two main components of the digital readout circuit shown in Figure 1 are a built-in self-test (BIST) architecture and a photon-counting circuit. A test controller, a Test Pattern Generator (TPG), and an On-Chip Response Analyzer (ORA) are the three main building blocks that make up the BIST architecture. This architecture's goal is to give the circuit a self-testing mechanism that can find and report any operational flaws or errors before the circuit is actually built. The photon counting circuit, on the other hand, is made up of four main building blocks: an array selector, a buffer, a Kogge Stone Adder (KSA), and a Parallel-In Serial-Out (PISO) register. This circuit's function is to count the photons that the circuit's input signal emits and turn them into a digital output signal.

During the testing process, the Test Controller, which is implemented as a Finite State Machine (FSM), receives a command to run a self-test. The FSM then deflects the incoming signal to the TPG signal, which produces a test pattern that is applied to the circuit. The ORA block subsequently examines the circuit's output in response to the test pattern and notifies the BIST controller of any operational errors or faults.

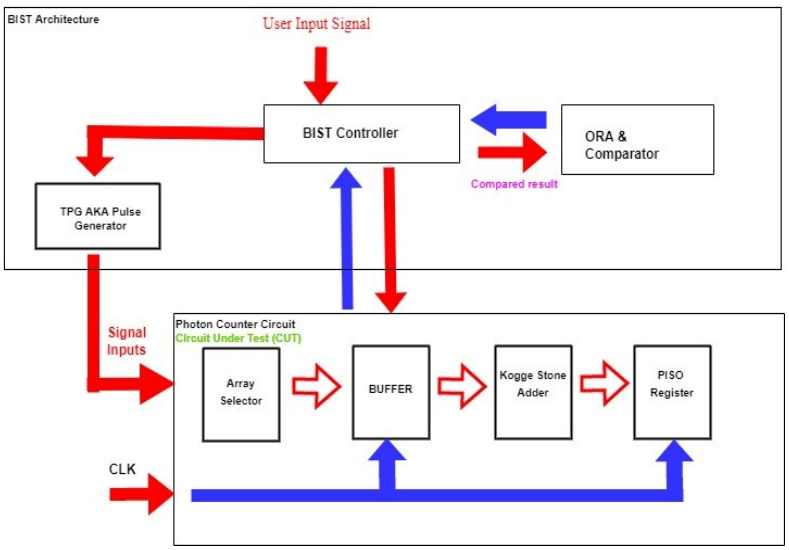

Figure 1. Block diagram of integrated readout circuit

As depicted in Figure 2, the circuit's data path unit (DPU) consists of a number of modules, including an array selector, a Built-In Logic Block Observation (BILBO) module, a KSA as adder, a PISO register, a ROM module, and a comparator. The 16 × 2 SPAD array, which detects photon emissions from the input signal, sends its input signals to the KSA block, which is in charge of summing them up. The PISO block receives the parallel input signal from the KSA block and transforms it into a serial output signal that can be seen at the circuit's output port. The carry-out signal from the KSA block is also connected to the output port to handle cases where the addition of both 16-bit inputs produces a 1-bit carry.

The inputs from the 16 × 2 SPAD module are synchronized using the buffer modules, which each have 16 D flip-flops. Due to the asynchronous nature of the input signals, the buffer modules make sure that the inputs are in sync with the clock signal, which is produced by the clock divider. To synchronize the operation of the buffer modules and the PISO block, the clock divider generates clocks with divisions of 16 and full periods, respectively. The D flip-flops in the buffer modules are edge-sensitive sequential logic, which means that only a rising or falling clock edge will cause an output change. The flip-flops are programmed to follow the rising edges of the A digital pulser module implemented in order to mimic the outputs generated by the 16 × 2 SPAD module. The output is randomized by the digital pulse module in order to simulate the circuit. This enables circuit testing and operation verification without requiring actual input signals from the SPAD module.

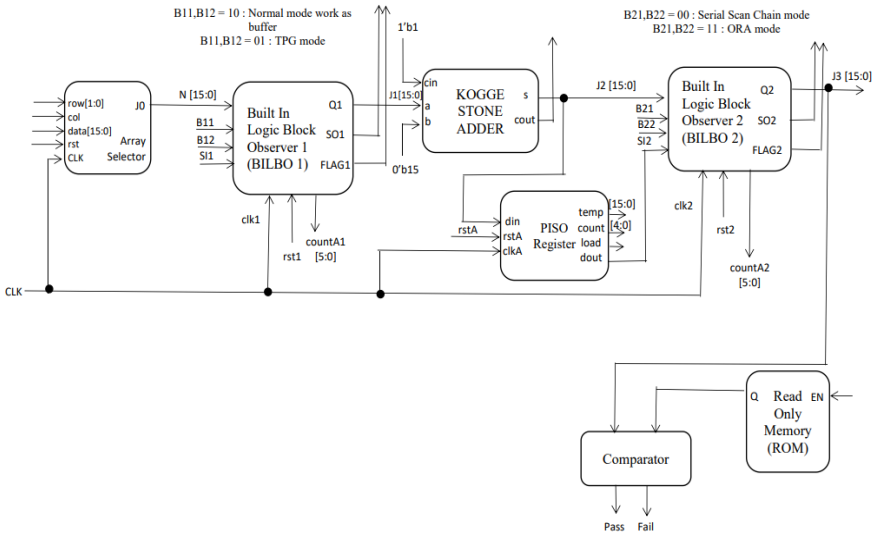

Figure 2. Data path unit (DPU) module

The DPU can function in two different modes: normal mode and test mode. The DPU operates as a digital readout circuit in normal mode. After passing through the buffer in BILBO 1, the KSA module, and the PISO register, the data flow N[15:0] from the array selector module. Finally, the output from the PISO register causes the serial scan chain mode BILBO 2 to output a 16-bit value. On the other hand, BILBO 1 functions as a test pattern generator in test mode, much like a typical linear feedback shift register (LFSR). In this mode, the generation of test patterns must begin with a logic value of "1" in the last bit of the data N[15:0] that enters BILBO 1. The KSA module, which is the circuit being tested, is where the test patterns created by BILBO 1 are then sent after passing through. In test mode, BILBO 2 operates as an output response analyzer.

The comparator will contrast a reference signature kept in the ROM module with the output response signatures produced by BILBO 2 during self-testing mode. The DPU can then use this information to check the circuit's functionality and find any errors or faults. As a result, the designed DPU described here should appear to be a flexible circuit that can run in both normal and test modes and be self-tested to ensure that it functions as intended.

The three devices CUT-1, CUT-2, and CUT-3 are intended to be tested by the Controller Unit (CU). The testing process involves running a sequence of tests, with each device being tested in turn. A device that fails a test is not permitted to move on to the following step in the data processing process until the error has been fixed. The CU has a reprogrammable timing system that makes it possible to regulate the number of test pattern generator cycles. This implies that the CU can be configured to generate a wide range of test patterns and run tests with various numbers of cycles. The output response analyser signals are extracted from the CU using a critical timing scheme. This suggests that the CU is able to analyse the output of the testing devices and can find any errors or problems that might be present.

3. EXPERIMENTAL RESULTS

BILBO can operate in four different modes to replace the buffer and PISO registers in the original data acquisition system, while KSA can perform fast addition in a single clock cycle. To ensure that the integrated circuit functions as intended, these modules were created to cooperate with one another. It might be possible to develop a system for photon counting or other data acquisition applications that is more effective and efficient by combining the capabilities of KSA and BILBO. While in testing mode, BILBO1 functions as a TPG to create new test patterns, while BILBO2 functions as an ORA to create signatures with the KSA module acting as the CUT, and this design makes up a BIST architecture.

To meet the requirements of building a full photon counting circuit, BILBO1 functions as a buffer in normal mode, while BILBO2 operates in serial scan mode, integrated with the KSA module and PISO register. The KSA design has been demonstrated to perform quick addition, as shown in Figure 3, where all of the bits can be added in a single clock cycle. As shown in the first red

rectangular box, when input a = 1 is added to input b = 0 adds to input Cin = 1 the result is output s = 2 and Cout = 0. For the second red rectangle box, input a = 3 adds to input b = 1 adds to input Cin = 1 1 results in output, s = 5, and Cout = 0. As seen in Figure 4, BILBO is in its default mode, acting as a buffer to produce the output values Q[15:0] from the input values D[15:0].

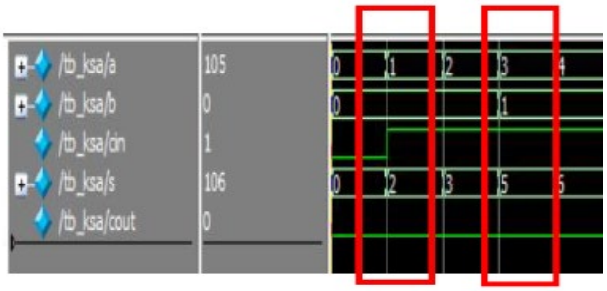

Figure 3. Simulation Results of KSA

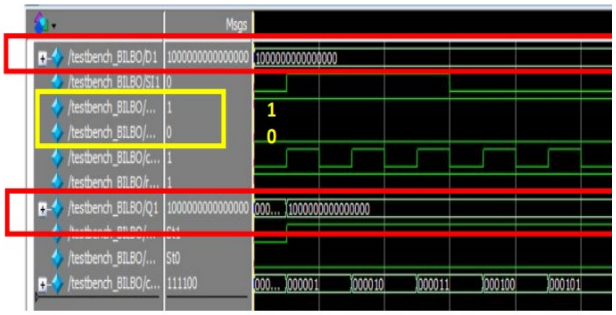

Figure 4. Simulation Results of BILBO in Normal Mode

As depicted in Figure 5, when BILBO is in serial scan mode, the inputs B1 and B2 are set to "00," the input SI in the BILBO receives a single bit value from the external source, and the bit value is inserted at the output Q[0] by pushing out the output Q[15] at each clock cycle. As a result, after 16 clock cycles, 16 bits of data from SI will be transmitted bit by bit to Q[15:0] data streams. The 16th bit of the value, Q[15], obtained from Q[15:0] data streams, is displayed in the output SO. BILBO is in TPG mode when it receives the input "01" because it generates test patterns every clock cycle as shown. The inputs of BILBO are initially set to "10" to scan in the seed value because LFSR needs a seed value to start generating test patterns. In its default mode, BILBO functions as a buffer to convert input values D[15:0] to output values Q[15:0]. It is demonstrated that BILBO is operating in ORA mode when the inputs are set to 11. Since LFSR requires a seed value to begin the operation, the inputs are initially set to "10." When inputs B1 and B2 in BILBO are set to "10," output Q[15:0] initially receives data streams from input D[15:0] because LFSR needs an input value to begin producing test patterns. BILBO changes to TPG mode after receiving the seed value at Q[15:0], receiving "01" as inputs, and begins to produce test patterns at each clock cycle as shown in Figure 6.

In the testing mode, BILBO1 and BILBO2 alternately generate test patterns and signatures up until the generated signatures are identical to the golden signature saved in the ROM module. The output signal PASS and displayPass will rise to "1" to indicate that the test has been passed. Once the test has been passed, the circuit will run a fresh test by entering a fresh test pattern and switching BILBO2 to normal mode. When the back to normal trigger is triggered, the circuit will switch from testing mode to normal mode.

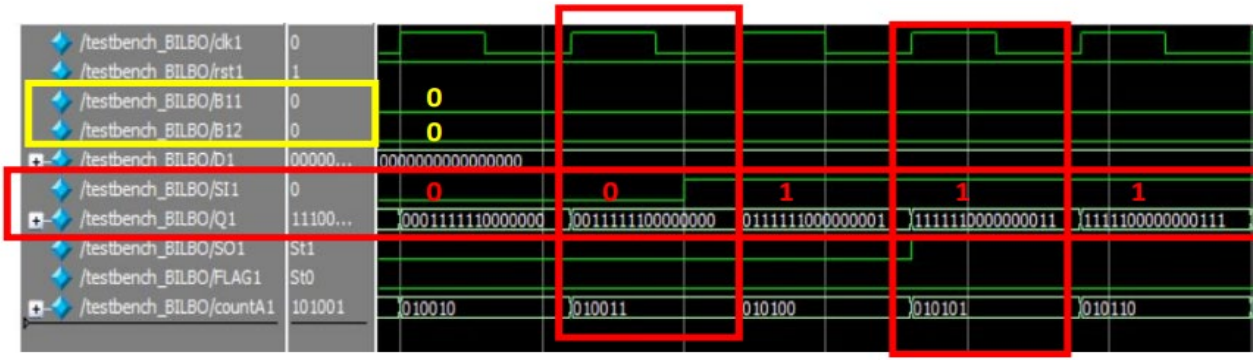

Figure 5. Simulation Results of BILBO in Serial Scan Mode

Placement and routing tasks are performed using ICC tools and a gate-level netlist is generated from DC synthesis via Synopsys. The used core utilization is 0.8. The slack time is met, according to timing reports for setup and hold time. In order to demonstrate the improvements over the prior design, the total cell area report and power report for the design are also obtained and examined in ICC. Comparing the current design to the previous one, which had cells with an area of 31244.88 µm2, the total cell area of 10218.70 µm2 has decreased by about 67% [3]. The power report reveals that the current design's power consumption has decreased to 1.7837 mW, which is about 38 % less than the previous design's power consumption of 2.8567 mW [3]. The suggested design can function at a 200 MHz minimum counting rate. The results are summarised in Table 1.

The DRC and LVS checks are also performed to ensure that the design is coherent between the schematic and

layout designs and that no critically violating paths are present. In addition, layout congestion analysis is done through Synopsys to show that the layout has moderate congestion only.

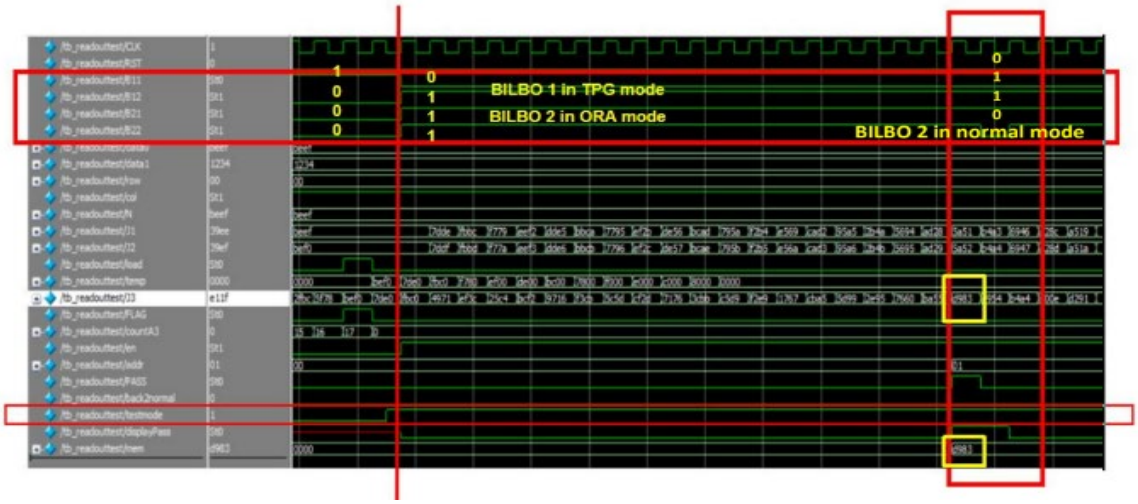

Figure 6. Simulation Results of Circuit Operating in Testing Mode

Table 1. Result Specifications

	Clock Periods (*ns*)	Setup Time Slacks	Hold Time Slacks	Total Power. (*mW*)	Total Power (μm^2)
1	5	0.75	0.26	1.96	10844.06
2	6	0.30	0.27	1.78	10218.70
3	7	0.50	0.27	1.52	10192.09

3. CONCLUSION

A crucial part of the photon counting array data processing on the chip that ensures the precision and dependability of the data produced by the chip is the self-test module. It runs a number of tests to find and fix errors, giving a way to confirm the chip's functionality and spot any deterioration in quality over time. Benefits of the self-test module include a reduction in the need for external testing tools, the ability to identify and isolate defective components, and a reduction in downtime. In conclusion, this project primarily makes use of a 16 x 2 SPAD array and has a scan-test module added. The BILBO design, which has four functional modes, is created to produce the desired results.

ACKNOWLEDGMENT

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