VOL. 25, NO. 2, 2026, 78-85
elektrika.utm.my
EISSN 3083-9394

ELEKTRIKA
Journal of Electrical Engineering

Low-Power Self-Biased Widlar Current Source for Sub-µA Biomedical Applications in 0.25 µm CMOS Technology

Jamilah Karim[1] and **Sohiful Anuar Zainol Murad**[2]

[1]Faculty of Electrical Engineering, Universiti Teknologi MARA, 40450 Shah Alam, Selangor.
[2]Micro System Technology, Centre of Excellence (CoE), Faculty of Electronic Engineering & Technology Universiti Malaysia Perlis, 02600 Arau, Perlis.

*Corresponding Author: jamilah329@uitm.edu.my

Abstract: This paper provides a systematic investigation of transistor sizing strategies for a self-biased Widlar current mirror topology to evaluate performance tradeoffs between subthreshold and saturation operation, focusing on ultra low current (< 1uA) bias generation suitable for biomedical applications**.** The first design (D1) employs aspect ratios that ensure all transistors operate in the subthreshold region, while the second design (D2) uses sizing that places all transistors in saturation. All simulations were performed using Eldo in Tanner EDA S-Edit environment, utilizing a 0.25 µm CMOS process. Simulation results confirm that both configurations generate output currents below 1 µA, making them suitable for low-power analog and biomedical circuits. The total power consumption for D1 is 3.5090 µW and for D2 is 3.5217 µW. D1 exhibits superior current matching and minimal temperature drift, whereas D2 achieves a higher PSRR (−71 dB), indicating stronger noise immunity. These results show that by adjusting the aspect ratio based on topology can help improve low-power current references despite changes in process, voltage, and temperature.

Keywords: Widlar current mirror, current mirror, low power current mirror, PSRR

Article History: received 14 July 2025; accepted 14 May 2026; published 31 August 2026
Digital Object Identifier 10.11113/elektrika.v25n2.767

1. INTRODUCTION

The increasing demand for ultra-low-power and high-precision analog circuits in biomedical and wearable sensor systems has created a need for compact, reliable current biasing solutions. In such systems, the stable operation of the current reference circuit over wide temperature ranges, enduring supply voltage variations, and consuming minimal silicon area and power is crucial. Typically, modern low power current mirror operates with power consumption ranging from 10nW to several microwatt, while maintaining reliable operation across temperature range from -40°C to 125°C. In addition, practical current reference circuits used in low-power sensor interfaces usually generate reference currents from nanoampere to the microampere range depending on the application requirements. Another important performance metric is the power supply rejection ratio (PSRR), which typically falls within -40 dB to -60 dB for low power analog bias circuits. These requirements leave conventional biasing circuits inadequate, especially under stringent Process, Voltage, and Temperature (PVT) variations [1]-[4]. Therefore, designing a compact current mirror capable of generating stable sub-microampere currents while maintaining competitive PSRR and robustness against PVT variations remains an important challenge in low-power analog circuit design.

Wearable biomedical systems and ultra-low-power sensor interfaces require precision biasing at sub-µA current levels to maintain signal integrity and minimize energy consumption. Conventional current mirrors, such as the basic two-transistor and Widlar configurations are widely used due to their simplicity, low power consumption, and compact area. However, these structures typically exhibit limited power supply rejection ratio (PSRR), low output impedance, and significant sensitivity to process, voltage, and temperature (PVT) variations, making them unsuitable for precision low-current biasing in advanced analog systems [5], [6]. These limitations cause undesirable fluctuations in bias current, especially when interfaced with analog front-ends in noisy or battery-variable environments. Furthermore, many bias generation circuits rely on external reference voltages or startup circuitry to ensure dependable operation, especially during power-on conditions. This adds to design complexity, silicon area, and power consumption, which can be prohibitive in system-on-chip (SoC) or wearable biomedical devices [7], [8]. Therefore, there is an increasing demand for a self-contained, self-starting, low-power bias current generator capable of providing a stable current despite supply and process variations, while maintaining high PSRR, output impedance, and reliable

operation without external references.

The goal of this project is to develop a self-biased Widlar current source capable of providing a stable current below 1 µA, suitable for low-power wearable devices. Achieving a high PSRR, high output impedance, and consistent performance despite variations in PVT is also part of the goal. Therefore, the self-biased Widlar configuration is chosen due to its simplicity, compactness, and energy efficiency, allowing for accurate sub-microampere current output without external bias references or startup circuitry. These features make it ideal for space-limited, ultra-low-power applications such as in biomedical and wearable applications, where reliability and power efficiency are vital.

The main contribution of this work is the systematic evaluation of transistor sizing for a self-biased Widlar topology to achieve stable sub-microampere current generation. Unlike many existing bias circuits that rely on auxiliary reference circuits or complex feedback structures, the proposed design maintains a simple architecture while achieving competitive PSRR and temperature stability. The comparative analysis between the subthreshold and saturation operating regions provides useful design insights for low-power analog circuits used in wearable and biomedical systems.

The remainder of this paper is organized as follows: Section 2 discusses existing current mirror designs, including Widlar and regulated cascode, FVF topologies, highlighting their strengths and limitations in low-power applications. Section 3 outlines the circuit design approach, simulation setup, and analysis techniques used to evaluate performance metrics such as PSRR, output impedance, and PVT robustness. Section 4 presents the simulation outcomes, including key performance graphs and comparisons with other biasing methods, supported by analysis of corner cases and load variations. Finally, Section 5 summarizes the main findings, confirms the effectiveness of the proposed self-biased current sink.

2. LITERATURE REVIEW

Various current mirror topologies have been developed to enhance key performance metrics, including current-matching accuracy, output resistance, voltage swing, power efficiency, and robustness to process and temperature variations. This chapter has reviewed prior work on current mirror circuits specifically designed for low-power applications, highlighting the advancements and trade-offs of each approach.

The cascode current mirror is a well-known topology commonly used in analog design due to its ability to greatly increase output impedance and enhance current mirroring accuracy by minimizing the effects of channel-length modulation. It works by stacking a transistor above the output device, which isolates it from variations in drain voltage and creates a high- output- resistance path. Ali and Hasan in [9] showed that these cascode current mirrors outperform simple current mirrors in current accuracy, especially under different load conditions, while Zhang and El- Masry in [10] improved cascode swing using a flipped- voltage- swing method, achieving over 112 GΩ output resistance and just 0.01% gain error at VDD ≈ 1 V. Muzira et al. in [11] expanded the design with a quasi-floating self-cascode output stage, reaching bandwidths over 1.3 GHz and Rout > 80 GΩ in low voltage nodes. Despite these improvements, traditional cascode current mirrors face limitations due to their restricted voltage headroom which require at least twice the saturation voltage ($2V_{DSsat}$) and add complexity in biasing and layout [12]. Recent advances have sought to overcome these issues through innovative architectural approaches. Pritty and Jhamb in [13] proposed a super-cascode current mirror for biomedical use, incorporating inverting amplifiers and level-shifting transistors to produce both positive and negative feedback. This design is implemented using 90 nm technology operates at 0.8 V, offering a bandwidth of 580.2 MHz, 3.963 nV/√Hz output noise and consumes only 11.879 µW. The design can also support a 50 GHz VCO at 300 µW. Nam et al. [14] addressed mismatch sensitivity in electrochemical sensors with a chopper-stabilized, dynamically matched gain boosted cascode current mirror fabricated in 0.18 µm CMOS, achieving 21.7 pA RMS input referred noise and just 1.13% mirroring error across 350 nA – 2.8 µA Iout and consume 287.9 µW power. Meanwhile, Julien et al. [15] designed a high- drive current mirror using a regulated cascode topology with nonlinear current conveyor (CCII)-based feedback, capable of handling 100 µA to 2 mA at over 90% power efficiency and less than 0.5% current copying error with a 100 ns response time. These studies highlight the cascode topology's adaptability in high speed, precision analog circuits. However, their complexity, voltage requirements, and power consumption limit their use in ultra-low power wearable or implantable devices. Therefore, while cascode current mirrors deliver exceptional performance for high frequency and moderate to high voltage applications, it is important to weigh the design complexity and voltage overhead against the intended use.

Thus, the flipped voltage follower (FVF) current mirrors have been developed as an alternative that emphasizes low-voltage operation and fast response. Various improvements to the FVF current mirror topology have been investigated to overcome the limitations of traditional current mirrors in low-power and low-voltage applications, especially for portable and biomedical devices. Unlike traditional or cascode current mirrors, the FVF structure leverages a negative feedback mechanism via a common-gate stage to fix the gate voltage of the output transistor, resulting in low input impedance, high output swing, and wide bandwidth under limited voltage headroom. Mallipeddi et al. [16] demonstrated a low-voltage current mirror based on the FVF topology with local negative feedback using a 180 nm CMOS process at 0.5 V supply, achieved a substantial improvement in output resistance from 700 kΩ to 401 MΩ without compromising bandwidth (2.4 GHz). Aloui et al. [17] further advanced the FVF design with a bulk-driven quasi-floating gate approach operating at 0.8 V supply, achieving 9.5 GΩ output impedance with only 79 µW power consumption and 99 µA output current, hence highlighting its suitability for low-power systems. Ghadiry et al. [18] introduced a self-biased FVF mirror to simplify external

circuitry while enhancing resilience against PVT variations, and Muzira et al. [11] added a quasi-floating self-cascode stage to extend bandwidth to 1.3 GHz. Despite these advancements, FVF current mirrors often need additional circuitry, such as bias generators or bulk-driving stages, which can complicate the design. Furthermore, floating node techniques may limit compatibility with standard CMOS flows. Nonetheless, the FVF topology remains a strong candidate for modern low-power analog circuits since it offers a compelling balance between simplicity, performance, and voltage efficiency. Although FVF current mirrors are ideal for low-voltage designs, they are not optimized for producing ultra-low currents in the nanoampere range.

Several studies have explored low-power current reference circuits using self-biased architectures to improve robustness against process, voltage, and temperature (PVT) variations. Aminzadeh et al. [7] proposed a nano-power self-biased CMOS voltage/current reference with a very compact structure, which eliminates the need for external bias circuitry; however, the simplicity of the design limit the optimization of parameters such as PSRR and output impedance. Similarly, Lefebvre and Bol [8] introduced an ultra-low-power current reference capable of generating nanoampere-level currents with strong PVT robustness, however the architecture involves a more complex design and therefore increase implementation overhead.

Motivated by these limitations, this work investigates a self-biased Widlar current mirror topology for low power operation. The proposed design focuses on achieving stable sub-microampere current generation while keeping the circuit simple and flexible. The Widlar current mirror is chosen because it can generate low currents in a compact and power-efficient by using source degeneration. Recent advances in Widlar current mirror topologies show their versatility for various low-power applications, including temperature sensing, current referencing, and strain detection. Widlar-based circuits are particularly attractive because they can generate ultra-low currents in compact layouts with minimal supply headroom. Kumar et al. [19] proposed a modified inverse-Widlar temperature sensor for high-performance multi-core processors, improving sensitivity through series resistors and achieving 1.81 mV/°C with ±1 °C INL from –20 °C to 100 °C. The design, implemented in 180 nm CMOS, only occupies 438 μm² and shows strong robustness to process variations. In biomedical and mechanical sensing, Roisina et al. [20] developed a low-power silicon strain sensor using four Widlar configurations, demonstrating a maximum sensitivity of 12.02 nA/με (gauge factor) with current subtraction, but consume higher power of 145 μW. Simpler resistor-based designs offered lower sensitivity and only used 28.6 μW of power. Aggarwal et al. [21] addressed the temperature drift issues of traditional Widlar current sources by combining a MOSFET–BJT pair in parallel, achieving a nearly constant 63 μA output with just 0.1 μA variation across –30 °C to 100 °C, outperforming the 24.87 μA drift of standard designs, and consume only 32.36 μW of power. For ultra-low-current applications, Sharroush and Abdalla [22] proposed nanoampere-range current sources using a subthreshold-modified Widlar structure and floating-gate MOSFETs, providing both analog tunability and digital programmability with <2 nA resolution. Liang et al. [23] developed a second-order, temperature-compensated, resistor-free Widlar current source in 0.18 μm CMOS, achieving a 16.9 ppm/°C temperature coefficient, a 1 μA reference current, and very low power consumption of 8.9 μW at a 1.3 V supply. The result highlights Widlar's suitability for thermally stable current generation. [24] emphasizes that Widlar's source-degeneration mechanism introduces local negative feedback, greatly enhancing output impedance and current stability while keeping low compliance voltage and simple design. Although its output impedance is lower compared to cascode or FVF-based current mirrors, the Widlar topology offers a good trade-off between complexity, accuracy, and power consumption, especially when combined with self-biasing, resistor tuning, or hybrid configurations. These results confirm that the Widlar topology is a strong candidate for modern low-power, high-precision applications such as biomedical implants and IoT sensors nodes.

3. METHODOLOGY

This chapter describes the circuit design approach, simulation setup and analysis used to evaluate the performance of the proposed widlar current mirror circuit.

3.1 Circuit Design Approach

The Self-Biased Widlar Current Mirror circuit shown in Figure. 1 is designed to generate very low output currents, (< 1 μA). The circuit contains two primary sections: the upper part is a PMOS current source mirror, while the lower part is an NMOS current sink arranged to become Widlar topology. These components work together to create a self-bias loop that can produce accurate reference and output currents independently of external biasing circuitry.

The PMOS current source comprises of two PMOS transistors; Mp1 and Mp2. Diode-connected Mp2 create a reference gate-source voltage. This voltage is mirrored onto Mp1, forming a standard current mirror. The current from Mp1 is sources to the NMOS section below. This setup ensures symmetrical biasing and allows current to flow from the positive supply rail VDD into the core Widlar structure. The Widlar NMOS current sink consists of two NMOS transistors that receive current from the PMOS mirror. Diode-connected Mn1 defines the reference current, Iref. The Mn2 transistor acts as the output branch and includes a source degeneration resistor, which introduces local negative feedback. The voltage drop across the degeneration resistor reduces the gate-source voltage of Mn2. Consequently, the output current Iout becomes significantly lower than Iref, enabling precise low-current generation. The relationship between Iref and Iout depends on the operating region of the transistors, either in subthreshold as in equation (l) or in saturation as in equation (2).

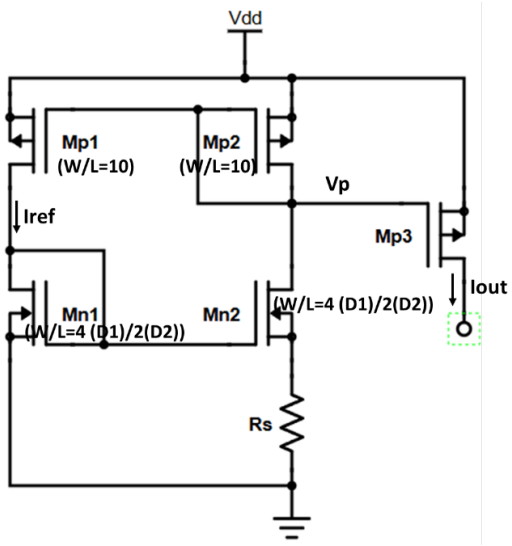


Figure 1. Self-Biased Widlar Current Mirror

If the transistor bias in subthreshold:

$$I_{out} = I_{ref}(-R_s I_{out}/nV_T) \quad (1)$$

And if transistor bias in saturation:

$$I_{out} = \frac{1}{2}\mu C_{ox}\,(W/L)\,(V_{GS} - V_{TH})^2 \quad (2)$$

3.2 Simulation Setup

Table 1 shows two different sets of transistor aspect ratios (W/L), that are examined: D1 ensures all transistors operate in the threshold region, while D2 all transistor bias in the saturation region. These aspect ratios were intentionally selected to investigate the influence of transistor operating regions on current stability, temperature sensitivity and PSRR performance for the same self-biased Widlar topology. The selection of the transistor sizes was guided by MOSFET current equations and further validated through simulation sweeps.

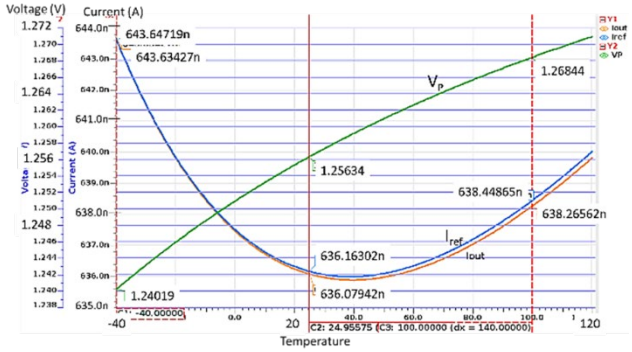
All simulations were performed using Eldo within the Tanner EDA S-Edit environment, utilizing a 0.25 µm CMOS process. The following analyses were conducted: first, DC sweeps—to evaluate the thermal stability of Iref and Iout over temperature (−40 °C to 120 °C), as well as the voltage drift of Vp with respect to temperature and VDD. Additionally, Iref, Iout, and Vp will also be evaluated across corners (TT, FF, SS) across standard temperature range. The second analysis is AC analysis, which is performed to extract the Power Supply Rejection Ratio (PSRR) and output resistance, Rout, across a frequency range of 10 Hz to 1 GHz.

Table 1. Aspect ratio of Transistors

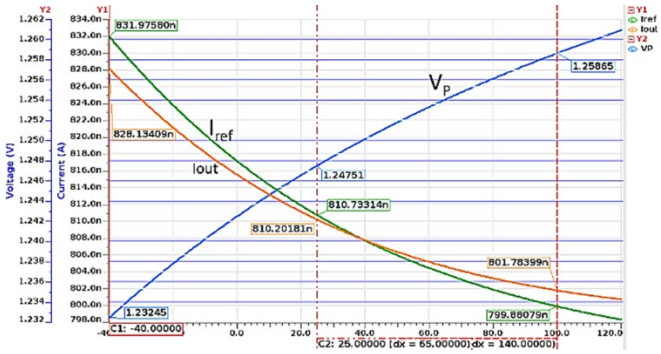
	W/L	
Devices	**D1**	**D2**
Mp1/Mp2	10	10
Mn1/Mn2	4	2
R	5k	5k

4. RESULT AND DISCUSSION

The simulations aim to validate the circuit's ability to maintain stable bias current, reject power supply noise, and operate reliably under process and temperature variations.



(a)



(b)

Figure 2. (a) Iref,Iout and Vp vs Temperature for D1 aspect ratio, (b) Iref,Iout and Vp vs Temperature for D2 aspect ratio.

Figure 2(a) and (b) shows the plot of Iref, Iout and Vp across temperature range from −40 °C to 120 °C for D1 and D2 respectively. Figure 2(a) demonstrates excellent current matching between Iref and Iout across all temperatures, with maximum error below 0.03%. This precision and thermal stability result from the exponential current-voltage behavior in subthreshold operation. Excellent matching is essential, as close matching directly affects analog bias reliability, temperature drift performance, and systematic offset error [25]–[28]. In addition, minimal deviation between Iref and Iout also confirms a well-matched W/L ratios between the reference and mirror transistors. In contrast, D2 demonstrates the current mismatch is minimal from 25 °C ~ 50 °C as shown in Figure 2(b), with the highest error recorded at −40 °C (0.46%). The circuit exhibits slightly higher thermal drift, indicating greater sensitivity to temperature fluctuations. However, all transistors operate in the saturation region, which is advantageous for higher speed and improved linearity. Table 2 shows the error percentage and the operating region for both aspect ratio D1 and D2. The error between Iout and I ref is calculated by using equation (3).

$$error = \frac{(I_{out} - I_{ref})}{I_{ref}} \times 100\% \quad (3)$$

Table 2. Iout error percentage and operating region for D1 and D2

	D1	D2
Iref–Iout Error (%)	0.002%–0.029%	0.065%–0.460%
Bias Region	All in Subthreshold	All in Saturation

Meanwhile, the bias voltage Vp exhibits a manageable drift of approximately 28 mV and 26 mV (equation (4)) across the full temperature range (−40 °C to 100 °C) for D1 and D2, respectively. The small drift in Vp in both designs indicates robust analog biasing behavior under PVT variations, and the similarity in drift values highlights the effectiveness of the self-biased configuration in both operating regions [29].

$$V_{drift} = V_p(100°C) - V_p(-40°C) \quad (4)$$

In general, <5% variation in current or voltage across standard temperature (−40 °C to 100 °C) is considered good [26], and <2% is considered excellent, especially for biomedical or subthreshold designs [28]. The maximum Iout error for D1 is ~1.2% (5) over full temperature from −40 °C to 100 °C confirms excellent temperature stability. This aligns with recent state-of-the-art current references demonstrating < 2% variation over −40°C to +85°C , such in [30], and over −40°C to +125°C in [31]. Meanwhile D2 demonstrate the maximum Iout error of 3.5%, over full temperature from −40 °C to 100 °C, shows good temperature stability.

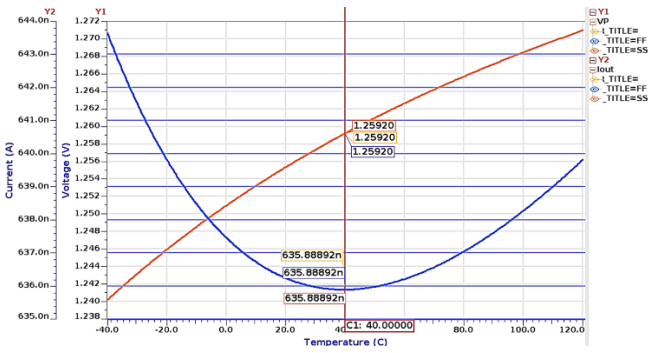
$$I_{(error)} = \frac{(I_{out}(T) - I_{out}(25°C))}{I_{out}(25°C)} \times 100\% \quad (5)$$

Table 3 displays the effect of supply voltage VDD on the bias voltage Vp and output current Iout for D1 and D2 across three temperatures: 40 °C, 25 °C, and 100 °C. The VDD range is 1.0-2.0 V. Both D1 and D2 show a consistent increase in Vp with increasing VDD, demonstrating good voltage tracking. However, Vp in D2 remains slightly lower than in D1 at all conditions. This behavior aligns with MOSFET theory, in which the gate voltage decreases slightly with increasing drain current due to increased overdrive in saturation mode [12]. Similarly, Iout increases nonlinearly with VDD in both designs, consistent with exponential current dependence in subthreshold (D1) and quadratic dependence in saturation (D2) [27]. Notably, D2 exhibits significantly higher Iout than D1 under the same VDD, reaching 1 µA at 2 V, while D1 remains below this threshold. This makes D1 preferable for ultra-low-power applications where minimizing static current is crucial [32], while D2 may be beneficial in scenarios requiring better PSRR and output drive strength. This shows that there is a clear trade-off between power efficiency and performance, as both Vp and Iout change with VDD.

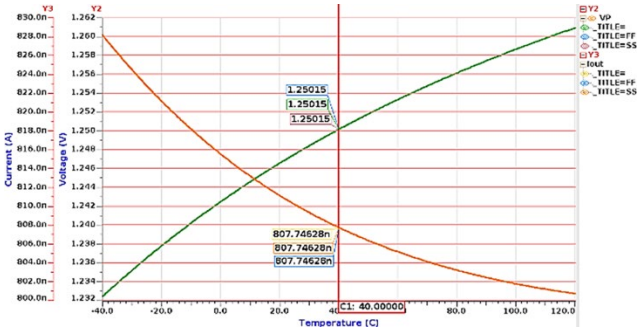
Table 3. Influence of VDD to Vp and Iout for D1 and D2

ASPECT RATIO D1						
	Vp (V)			Iout (µA)		
V_{DD} (V)	at -40°C	at 25°C	at 100°C	at -40°C	at 25°C	at 100°C
1	0.503	0.521	0.537	0.000	0.000	0.000
1.2	0.678	0.697	0.712	0.256	0.273	0.293
1.4	0.862	0.880	0.894	0.385	0.394	0.408
1.6	1.050	1.067	1.080	0.514	0.515	0.523
1.8	1.240	1.256	1.268	0.644	0.636	0.638
2	1.432	1.448	1.459	0.773	0.757	0.753
ASPECT RATIO D2						
	Vp (V)			Iout (µA)		
V_{DD} (V)	at -40°C	at 25°C	at 100°C	at -40°C	at 25°C	at 100°C
1	0.501	0.519	0.536	0.000	0.000	0.000
1.2	0.673	0.692	0.707	0.302	0.318	0.335
1.4	0.856	0.873	0.887	0.473	0.478	0.487
1.6	1.043	1.059	1.071	0.649	0.643	0.643
1.8	1.232	1.248	1.259	0.828	0.810	0.802
2	1.424	1.438	1.448	1.009	0.979	0.962

Figure 3(a) and (b) shows the output current Iout and bias voltage Vp across a temperature range (−40 °C to 120 °C) for three different process corners: Typical-Typical (TT), Fast-Fast (FF), and Slow-Slow (SS). The curves corresponding to each process corner show minimal spread, highlighting the strong insensitivity of both Iout and Vp to process variations. At 40 °C, the convergence of all three curves at the same operating point in Vp and Iout for D1 and D2 confirms that the circuit compensates the process excellently. This level of stability is essential for precision analog and low-power sensor applications, where variations in bias conditions can degrade performance. The results confirm that the design successfully minimizes sensitivity to PVT (process, voltage, and temperature) variations, a key challenge in subthreshold and ultra-low-power operation.



(a)

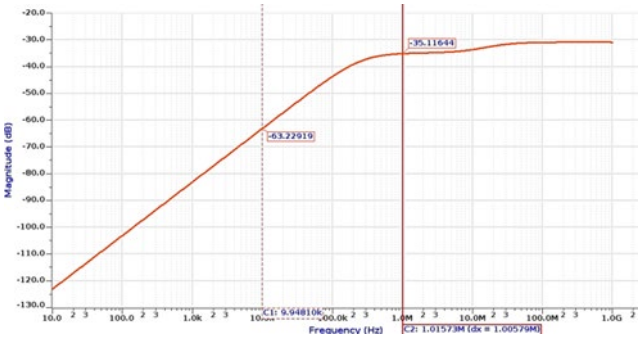


(b)

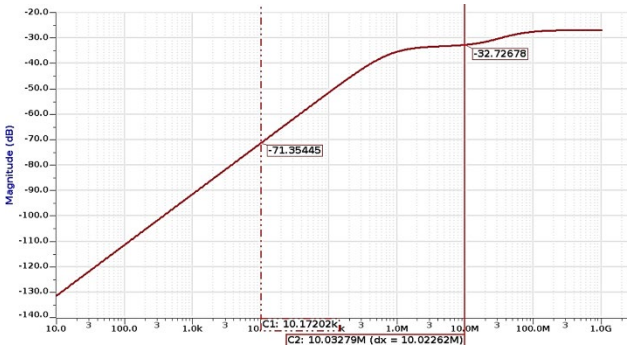
Figure 3. The output current Iout and bias voltage Vp across a wide temperature range (−40 °C to 120 °C) under three different process corners: Typical-Typical (TT), Fast-Fast (FF), and Slow-Slow (SS) for (a) D1 and (b) D2.

Figure 4 shows the PSRR for aspect ratio D1(a) and D2(b). As observed in the Figure 4, D1 (higher aspect ratio) exhibits PSRR of –63 dB at 10 kHz. Conversely, D2 (smaller aspect ratio) shows improved PSRR of –71 dB. This trade-off arises because higher gm associated with larger W/L ratios increases the sensitivity of the bias node to supply variations, thereby degrading PSRR performance [25], [33].

However, the PSRR of the proposed circuit with both aspect ratio indicates strong suppression of supply ripple across both low and moderate frequency ranges. This level of rejection is particularly significant in biomedical and wearable applications, where the analog front-end and sensor readout circuits are susceptible to supply noise originating from battery ripple, wireless transceivers, and switching regulators. The high PSRR at 10 kHz ensures effective rejection of low-frequency disturbances, which overlap with key physiological signals (e.g., EEG, ECG, and pressure). Meanwhile, the −35 dB and -32 dB attenuation at 1 MHz provides sufficient isolation from high-frequency switching noise commonly generated by on-chip or nearby DC-DC converters. Compared to state-of-the-art designs in the biomedical domain, the achieved PSRR is highly competitive. Previous works report PSRR in the range of −40 dB to −60 dB for low-power reference and bias circuits [28],[34]–[36], which are often sufficient to preserve signal integrity in wearable and implantable systems. Therefore, the obtained PSRR levels confirm that the proposed circuit offers robust noise immunity and is well suited for integration in low-power, noise-sensitive biomedical signal acquisition platforms.



(a)



(b)

Figure 4. PSRR (Power Supply Rejection Ratio) for (a) D1 and (b) D2.

The achievable output impedance for D1 is 73 MΩ, notably higher than the 30 MΩ observed for D2. This suggests that D1 provides superior current source characteristics at low frequencies, which is advantageous for maintaining precision in analog applications with ultra-low power consumption. The total power consumption for D1 is 3.5090 µW, compared to 3.5217 µW for D2. The low power consumption of the proposed circuit is mainly attributed to the self-biased Widlar architecture and the operating region of the transistors.In the D1 configuration, subthreshold operation enables the generation of very small currents with minimal bias voltage, thereby reducing static power consumption. In addition, the self-biasing structure removes the need for external reference or startup circuits, allowing a compact implementation with reduced overall power usage.

Table 4 compares the performance of the proposed self-biased Widlar current source with several recently reported low-power current reference circuits. Although some designs achieve lower power consumption, they typically require more complex architectures or operate at extremely small current levels. The proposed circuit provides a balanced trade-off between circuit simplicity, current stability, and noise immunity. In particular, the D2 configuration achieves a PSRR of −71 dB, which is competitive with recently reported low-power reference circuits while maintaining a simple four-transistor self-biased structure.

Table 4. Performance comparison with existing low-power current reference circuits

Ref	Tech.	I_{out}	V_{DD}	Diss. Power	PSRR	Key Feature
[28]	180 nm	10 µA	1.2V	4.2µW	−52 dB	Low-voltage CMOS current reference
[34]	180 nm	1 µA	1.8V	180 nW	−65 dB	Self-biased current reference
[35]	180 nm	1.2 µA	1.5V	110 nW	−60 dB	All-MOS current reference
[30]	22 nm	2.5 nA	0.8V	1.5 µW	−55 dB	Ultra-low current reference
This Work (D1)	**0.25 µm**	**0.75 µA**	**1–2V**	**3.51 µW**	**−63 dB**	**Subthreshold self-biased Widlar**
This Work (D2)	**0.25 µm**	**0.98 µA**	**1–2V**	**3.52 µW**	**−71 dB**	**Saturation-biased Widlar**

5. CONCLUSION

A self-biased Widlar current mirror circuit has been successfully designed and investigated. The influence of two aspect ratios on key performance parameters was analysed: one operating in the subthreshold region and the other in saturation. The subthreshold-bias setup (D1) demonstrated superior current matching and thermal stability, making it suitable for ultra-low-power applications. Conversely, the saturation-bias configuration (D2) provided improved power supply rejection ratio (PSRR), which is beneficial for noise-sensitive environments. Both configurations maintained output currents below 1 µA over a broad range of supply voltages and temperatures. These findings confirm that careful transistor sizing can tune the circuit to balance power, stability, and noise rejection. Therefore, validating that the self-biased Widlar current mirror is robust and flexible for low-power analog design.

ACKNOWLEDGMENT

The authors would like to express their sincere gratitude to Universiti Teknologi MARA for providing the academic environment, facilities, and continuous support throughout this research. The authors also gratefully acknowledge Emerald Systems Sdn. Bhd. for the opportunity and platform that enabled the successful completion of this study.

REFERENCES

[1] M. H. Shabaan, A. R. A. B. Shahrani, and M. A. El-Aasser, “A taxonomy of low-power techniques in wearable electronics,” Electronics, vol.13, no. 15, p. 3097, 2024. [Online]. Available: https://www.mdpi.com/2079-9292/13/15/3097

[2] C. L. Chen, T. H. Lee, and Y. C. Wang, “An ultra-low power amplifier for wearable and implantable biomedical sensors,” Microelectronics Journal, vol. 94, pp. 1–7, 2024. [Online]. Available: https://www.sciencedirect.com/science/article/abs/pii/S0167931719302114

[3] M. R. Qureshi et al., “A wide range temperature stable integrated current reference,” ResearchGate, Mar. 2025. [Online]. Available:https://www.researchgate.net/publication/4050455

[4] Y. Lin and C. H. Chen, “A current reference with wide temperature operation range,” IET Electronics Letters, vol. 60, no. 3, pp. 150–152, 025. [Online]. Available: https://ietresearch.onlinelibrary.wiley.com/doi/full/10.1049/ell2.12455

[5] S. S. Rajput and S. S. Jamuar, “Low voltage analog circuit design techniques,” IEEE Circuits and Systems Magazine, vol. 2, no. 1, pp. 24-42, 2002.

[6] M. P. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th ed. Hoboken, NJ, USA: Wiley,2009.

[7] M. Aminzadeh, A. G. Rezaei, and M. Sawan, “A self-biased nano-power 4-transistor CMOS voltage/current reference,” Electronics Letters, vol. 56, no. 4, pp. 222–224, Feb. 2020.

[8] T. Lefebvre and D. Bol, “A 2.5-nA area-efficient and PVT-robust current reference in 22nm FDSOI CMOS,” arXiv preprint, arXiv:2401.12800, 2024.

[9] A. M. A. Ali and H. M. Hasan, “Design of low-voltage low-power cascode current mirror with improved performance,” in Proc. IEEE Int. Conf. on Computing, Analytics and Security Trends (ICCAST), 2018, doi:10.1109/CAIS.2018.8442037.

[10] X. Zhang and E. El-Masry, “Improving output voltage swing in cascode current mirrors,” Circuits, Systems, and Signal Processing, 2023, doi:10.1007/s00034-023-02293-7.

[11] K. Muzira, S. Chander, and S. K. Sinha, “Low voltage high bandwidth FVF current mirror using quasi floating self-cascode output stage,” Analog Integrated Circuits and Signal Processing, vol. 119, pp. 15–27, 2023, doi:10.1007/s10470-023-02205-4.

[12] B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001.

[13] P. Pritty and M. Jhamb, “Design of extremely low power, high compliance and low noise current mirror,” Computers and Electrical Engineering, vol. 122, p. 110015, 2025.

[14] K. Nam, G. Choi, H. Kim, M. Yoo, and H. Ko, “A potentiostat readout circuit with a low-noise and mismatch-tolerant current mirror using chopper stabilization and dynamic element matching for electrochemical sensors,” Applied Sciences, vol. 11, no. 18, p. 8287, 2021. [Online]. Available: https://doi.org/10.3390/app11188287

[15] M. Julien, S. Bernard, F. Soulier, V. Kerzérho, and G. Cathébras, “A power-efficient high-drive current mirror combining a regulated cascode topology with a non-linear CCII-based feedback,” Electronics, vol. 13, no. 8, p. 1556, 2024. [Online]. Available: https://doi.org/10.3390/electronics13081556

[16] A. Mallipeddi, G. V. P. Anjaneyulu, P. B. Desavathu, and Y. M. Rao, "Design of low voltage high output resistance current mirror," Int. J. Exp. Res. Rev., vol. 30, pp. 57–62, 2023, doi: 10.52756/ijerr.2023.v30.006.

[17] M. Bchir, I. Aloui, and N. Hassen, "A bulk-driven quasi-floating gate FVF current mirror for low voltage, low power applications," Integration, the VLSI Journal, vol. 74, pp. 45–54, Sep. 2020, doi: 10.1016/j.vlsi.2020.04.002.

[18] M. Ghadiry, M. Sharifkhani, and A. Fotowat-Ahmady, "A self-biased flipped voltage follower current mirror," AEÜ – Int. J. Electron. Commun., vol. 122, 2020, doi: 10.1016/j.aeue.2020.153239.19] A. Kumar, A. Sahu, A. Dwivedi, and S. P. Tiwari, "Design of a Sensitivity-Improved On-Chip Temperature Sensor Based on Inverse-Widlar Architecture," in Advances in VLSI, Communication, and Signal Processing, Springer, Singapore, 2023, pp. 345–355, doi:10.1007/978-981-99-4495-8_30.

[20] N. Roisina, T. P. Delhaye, N. André, J.-P. Raskin, and D. Flandre, "Low-power silicon strain sensor based on CMOS current reference topology," arXiv preprint, arXiv:2201.13352v2, Jan. 2022.

[21] B. Aggarwal, Y. Arora, and J. K. Dhonac, "Bandgap current reference using Widlar current source," Indian J. Eng. Mater. Sci., vol. 27, no. 4, pp. 934–938, Aug. 2020.

[22] S. M. Sharroush and Y. S. Abdalla, "Proposed wide dynamic-range controllable current sources," Ain Shams Engineering Journal, vol. 14, p. 102127, 2023.

[23] Y. Liang, H. Zhao, and Y. Wang, "A Second-Order Temperature-Compensated CMOS Current Reference Without Resistors," Journal of Circuits, Systems and Computers, 2024, doi:10.1142/S021812662450042X.

[24] R. S. Alomari and A. Yakovlev, "A Survey of Current Mirror Techniques for Low-Power CMOS Circuits," Electronics, vol. 12, no. 3, pp. 1–22, 2024, doi:10.3390/electronics12030566.

[25] A. S. Sedra and K. C. Smith, Microelectronic Circuits, 7th ed., Oxford University Press, 2015.

[26] R. J. Baker, CMOS: Circuit Design, Layout, and Simulation, 3rd ed. Hoboken, NJ, USA: Wiley-IEEE Press, 2010.

[27] P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, 3rd ed. Oxford Univ. Press, 2012

[28] M. Yazdi and A. K. Sangaiah, "A low-voltage, low-power CMOS current reference with high power supply rejection and low temperature coefficient," Microelectronics Journal, vol. 61, pp. 50–58, Jan. 2017, doi: 10.1016/j.mejo.2016.12.003

[29] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations," IEEE Journal of Solid-State Circuits, vol. 12, no. 3, pp. 224–231, Jun. 1977. doi: 10.1109/JSSC.1977.1050677.

[30] V. Lefebvre and D. Bol, "A 2.5-nA area-efficient temperature-independent 176-/82-ppm/°C CMOS-only current reference in 0.11-µm bulk and 22-nm FD-SOI," IEEE Journal of Solid-State Circuits, accepted May 2024. [Online]. Available: https://arxiv.org/abs/2406.04741

[31] T. Borejko and W. A. Pleskacz, "Design of voltage–current reference source in CMOS technology," Electronics, vol. 13, no. 21, article 4212, 2024, doi: 10.3390/electronics13214212

[32] A. Wang, B. H. Calhoun, and A. Chandrakasan, Sub-threshold Design for Ultra Low-Power Systems. Springer, 2006.

[33] A. J. Lopez-Martin, S. Celma, J. Ramirez-Angulo, and R. G. Carvajal, "Low-voltage super class AB CMOS current buffer," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 51, no. 2, pp. 63–67, Feb. 2004.

[34] C. Chen, J. Hu, and H. Yu, "A 180nW 18.5ppm/°C self-biased current reference with PSRR enhancement technique in 180nm CMOS," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 12, pp. 3562–3566, Dec. 2020, doi: 10.1109/TCSII.2020.2978382.

[35] D. Jeong, H. Kim, and Y. Kim, "A 110-nW All-MOS Current Reference With Enhanced Line Sensitivity and PSRR," IEEE Solid-State Circuits Lett., vol. 3, pp. 282–285, 2020, doi: 10.1109/LSSC.2020.3010184.

[36] S. S. Saponara et al., "Low-power, low-noise analog front-end for wearable biomedical sensors," Electronics, vol. 10, no. 3, article 345, Feb. 2021, doi: 10.3390/electronics10030345.