

ZnO Thin Film Transistor: Effect of Traps and Grain Boundaries

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Abstract: Recently ZnO has drawn a lot of attention in semiconductor industry due to its interesting features. High exciton binding energy, high resistivity against radiation, high breakdown voltage, low temperature deposition are some of the interesting features of this material. Zinc oxide TFT device gains an increasing interest for its potential in sensing applications due to its biocompatibility, chemical stability and simple fabrication process with various methods and high surface-to-volume ratio. However, ZnO TFT devices from previous work exhibited poor I_{ON} and field effect mobility. This work investigates the cause of its poor performance by focusing only two factors: traps and defects in the channel and grain boundary. The work was performed in Silvaco TCAD 2D simulator. It was found that a single grain boundary in the channel causes a reduction of the I_{ON} by 95%. The effect in the I_{ON} is less severe when traps and defects were introduced in the ZnO channel. The results can assist in optimizing the TFT device performance for sensing applications.

Keywords: TCAD simulation, TFT, ZnO.

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1. INTRODUCTION

Nowadays, thin film transistor (TFT) structure is gaining interest among academic and industry researchers not only for display applications but also as a sensing device. Various types of organic and inorganic materials were implemented in TFT structure as the active channel for chemical, biological, optical, magnetic, radioactive and other sensors by controlling the transport of charge carriers or emission of photon [1-4]. Although TFT structure and its operation principles are the same as MOSFET but the fabrication involved is much simpler and hence more cost-effective.

One of the semiconductor materials which is widely researched in TFT structure is zinc oxide, ZnO. Due to its wide band gap at approximately 3.3 eV, it makes an interesting material for optical and sensor applications [5]. ZnO has the potential in the TFT technology for application in flexible and large-area electronics. Moreover, ZnO is attractive because of its relatively high charge carrier mobility and visual transparency [5]. These materials could build the foundation of thin film transistor technology for application in flexible and large-area electronics. Besides that, ZnO has excellent chemical and thermal stability and can be well oriented on various substrates [6].

Due to the ease of TFT structure and ZnO biocompatibility, ZnO TFT chemical sensor is an interesting device to be studied. However, ZnO film is known to be polycrystalline thin film [7]. The film has defects and grain boundaries which can impede the electron flow. Therefore, this work studies the effect of

these defects and grain boundaries to the electrical characteristics of the ZnO TFT using basic device simulation. This is important in order to understand the key factors to further improve the TFT performance for chemical sensor applications.

2. METHODOLOGY

The ZnO TFT was designed by using SILVACO DevEdit tools virtually [8]. The important part of the design using DevEdit is meshing the structure. Meshing function is to get the precise and accurate points for characterization. Meshing in SILVACO allow the user control the detail of structure through multiple criteria; include material type, quality change, location or relative location [8].

The ZnO TFT structure is designed based on the work of S.M.Sultan *et al* [9]. The parameters of thin film transistor that were used are $10\mu\text{m}$ and $5\mu\text{m}$ for width and length respectively. The p-type substrate is highly doped which act as gate for this bottom gate structure. The doping concentration for the highly-doped bottom gate silicon is $1 \times 10^{20} \text{ cm}^{-3}$ which degenerate the silicon gate into semiconductor level comparable to metals. The doping concentration of ZnO layer is set as $1 \times 10^{16} \text{ cm}^{-3}$. Figure 1 shows the ZnO TFT structure.

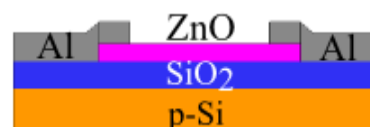


Figure 1. Schematic diagram of the TFT structure



Figure 2. Fabrication steps virtually in two-dimensional SILVACO TCAD Tools (a) highly doped silicon as bottom gate (b) silicon oxide (c) zinc oxide thin film and (d) Al electrodes as the source and drain

Figure 2 shows the step by step fabrication process of the TFT structure. The virtual fabrication step starts from the substrate of p-type silicon followed by the second layer which is SiO₂ with 200 nm of thickness. The channel layer of this structure is zinc oxide which is connected to the source and drain layer with Aluminium material.

The analysis of the effect of defects and grain boundary was performed with the aid of numerical simulations using the Silvaco Atlas device simulator [8]. A 2D coupled Poisson's drift-diffusion model was used to investigate the TFT operation. In addition, model for carrier emission and absorption processes proposed by Shockley-Read-Hall (SRH) was used to reflect the recombination phenomenon within the device. The simulations were performed at room temperature.

The transistor parameters were extracted by using ATLAS commands. The I_D/V_D and I_D/V_G curves with different gate voltages were plotted in ATLAS. After obtaining the IV characteristics, the ZnO channel was introduced with various types of defects such as traps and a single grain boundary (GB) in the middle of the channel. Defects were introduced using the command *defect* in the simulation tool with trap densities of $7.5 \times 10^{18} \text{ cm}^{-3}$. In all

3. RESULTS & DISCUSSION

In the simulations, it was assumed that the interface of SiO₂/ZnO layer is free of interface charges. The defects are only applied to the active layer of ZnO TFT. Figure 3 shows the semilogarithmic plot of the I_D-V_G characteristics of the ZnO TFT with three different conditions; crystalline ZnO TFT, ZnO channel with traps in the channel and with a single grain boundary in the ZnO channel. Crystalline ZnO TFT shows a threshold voltage measured to be 1.36 V. At $V_G = 0 \text{ V}$, the I_D is $8 \mu\text{A}$ and maximum current of $14.8 \mu\text{A}$ is obtained at $V_G = 5 \text{ V}$. This maximum current of I_D at $V_G = 5 \text{ V}$ is termed as I_{ON} in this paper.

When traps were introduced in the channel with trap densities of $7.5 \times 10^{18} \text{ cm}^{-3}$, the threshold voltage was

shifted positively to 2.83 V. The I_{ON} reduced to $5.5 \mu\text{A}$ at $V_G = 5 \text{ V}$. Meanwhile when a single grain boundary was introduced in the ZnO channel, the threshold voltage shifted positively to 2.3 V. However, I_{ON} reduced drastically to $0.17 \mu\text{A}$.

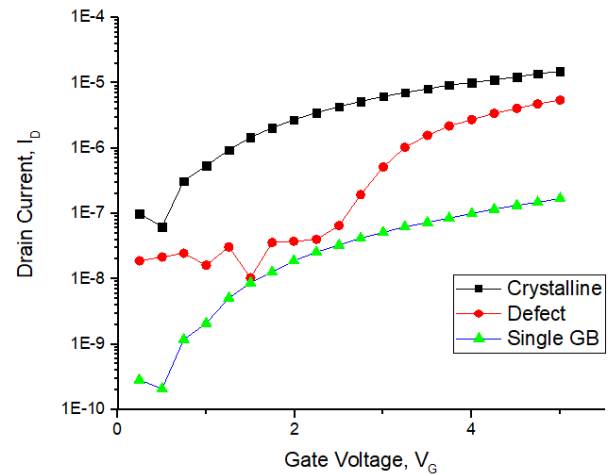


Figure 3. Semilogarithmic plot of the I_D-V_G characteristics of the ZnO TFT with three different conditions

Figure 4 shows the contour plot of the electron flow in the ZnO TFT channel and its concentrations during these three conditions. For crystalline ZnO TFT, the depletion region under the drain electrode is more gradual at $V_D = 1 \text{ V}$. However, when defects were introduced inside the ZnO channel, the depletion area under the drain region which is highlighted in yellow has increased. This indicates, more voltage is needed to ensure channel conductivity which results in higher threshold voltage as shown in the I-V characteristics earlier.

Figure 4(c) shows the contour plot when a single GB defined in the middle of the channel parallel to the ZnO film thickness and perpendicular to the direction of carrier propagation from source to drain. The GB is modeled as a thin layer (a few atomic layers) having defect states with Gaussian distribution as defined in Ref [8,10]. From the contour plot, depletion region starts to be visible after the GB region. It was reported in F.M.Hossein *et al* work that a double Schottky barrier is formed in the GB which impede the flow of electrons. As a result, when the threshold voltage is achieved, carriers transport over the GB will follow the thermionic emission process [7]. From the IV characteristics, the threshold voltage, V_{TH} increases by 70% and the drain current, I_D decreases by 95% when a single GB defined in the channel.

The increase of V_{TH} and the decrease in I_D affect the switching performance of the device. However, in P.Yasaei *et al* work, GB can enhance the sensitivity of the gas-sensing behaviour in graphene [11]. It was shown that the sensitivity of an isolated GB is x 300 times higher than that of a single graphene grain and much larger than that of polycrystalline graphene sensors [11].

Meanwhile when traps and defects were defined in the ZnO channel, the current decreases by only 63% from the crystalline ZnO. ZnO thin film is well-known for its inherently high dope of n-type materials which always attributed to the oxygen vacancies [12]. These oxygen

vacancies could be the possible source of traps. The oxygen vacancies in ZnO are in three states: V_O state which has captured two electrons and is neutral with respect to the lattice, the single ionized state V_O^+ and the V_O^{++} which did not trap any electrons and is doubly positively charged. V_O^+ defect sites are found mostly at the surface of ZnO [13]. These trap sites can cause the threshold voltage to shift positively because more electrons needed to be pumped into the active layer to overcome the trapped electrons. Consequently, higher electric field is needed in the channel layer.

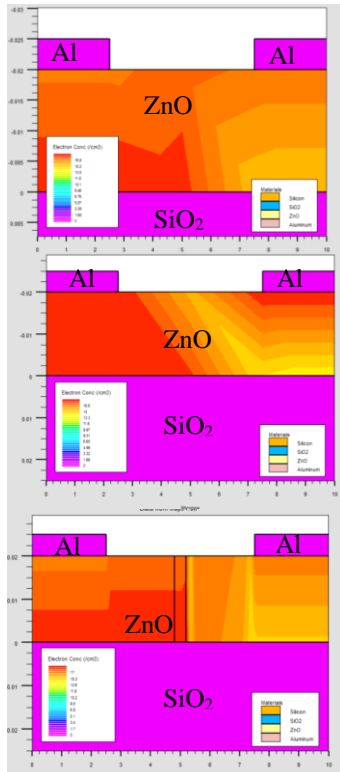


Figure 4 Contour plots of the electron concentration at different situations (a) crystalline ZnO TFT (b) when traps are introduced in the ZnO channel (c) when a single grain boundary introduced in the ZnO channel

3. CONCLUSIONS

Our TCAD simulations verify that the type of disorder (defect sites or grain boundary) is a determining factor in ZnO TFT performance. We have shown that a single GB in the active channel can have a large effect on the drain current. Meanwhile a high amount of defects in the ZnO channel cause a current decrease of 63% compared to 95% when a GB is defined in the channel. Therefore, it is important to determine the type of ZnO deposition process to be used in order to minimize grain boundaries in order to achieve optimized TFT performance for sensing applications.

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